

ZFWAA

Dione 10FU/10FUT

LA-B412P REV 0.2 Schematic

Intel Processor (Ivy Bridge) + PCH (Panther Point)

2014-01-02 Rev 0.2

| | | | | | | |
|--|--------------------|-----------------|------------|--------------------------|-----------------------------|---------------|
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| RTC CKT. | page 16 |
| DC/DC Interface CKT. | page 32 |
| Power Circuit DC/DC | page ?? |
| GCLK SLG3NB244VTR | page 26 |

Intel CPU
Ivy Bridge
17W
BGA-1023
31mm*24mm
page 5,6,7,8,9,10

Memory BUS(DDR3L)
Dual Channel
1.35V DDR3L 1600 MT/s

204pin DDR3-SO-DIMM X2
BANK 0, 1, 2
page 11,12

LVDS & eDP Conn.
page 13

CRT Conn.
page 14

HDMI Conn.
page 15

RJ45 Conn. RTL8106E & 8111G
PCIe port 1
page 27
USB Left
USB20 port 2
page 27

To sub-board
(JLAN)

Sub Boards

LS-B301P
LED/B
page 31

LS-B302P
Power Button/B
page 31

LS-B303P
LAN+USB/B
Audio Combo Jack
page 27

LS-B304P
CardReader/TP/LID B
page 31

SPI ROM
(8MB)
page 16

LPC BUS
3.3V 33 MHz

HD Audio
3.3V 24MHz

KB9012
page 30

TPM
NPCT650
page 26

HDA Codec
ALC233-VB2
page 29

Touch Pad+LID/B
page 31

To sub-board
(JCARD)

LED/B
page 31

To sub-board
(JLED)

Int.KBD
page 31

FDI X8
2.7GT/s

DMI X4
5GT/s

Intel PCH
Panther Point
FCBGA-989
25mm*25mm
page 16,17,18,19,20,21,22,23,24

USB30 1x
5V 5GT/s
USB20 2x
5V 480MHz

USB Right 3.0*1+2.0*1
USB30 port 0,1
USB30 port 1
page 28

USB20 2x
5V 480MHz

Int. Camera
USB port 11
page 13
Touch Screen
USB port 8
page 13

PCIe Gen1 1x
1.5V 5GT/s
USB20 1x
5V 480MHz

NGFF Slot 1 - WLAN & BT
PCIe port 2 & USB port 9
page 25

PCIe Gen1 1x
1.5V 5GT/s

Card Reader
PCIe port 4
page 31

To sub-board
(JCARD)

SATA Gen3 1x
5V 6GHz(600MB/s)

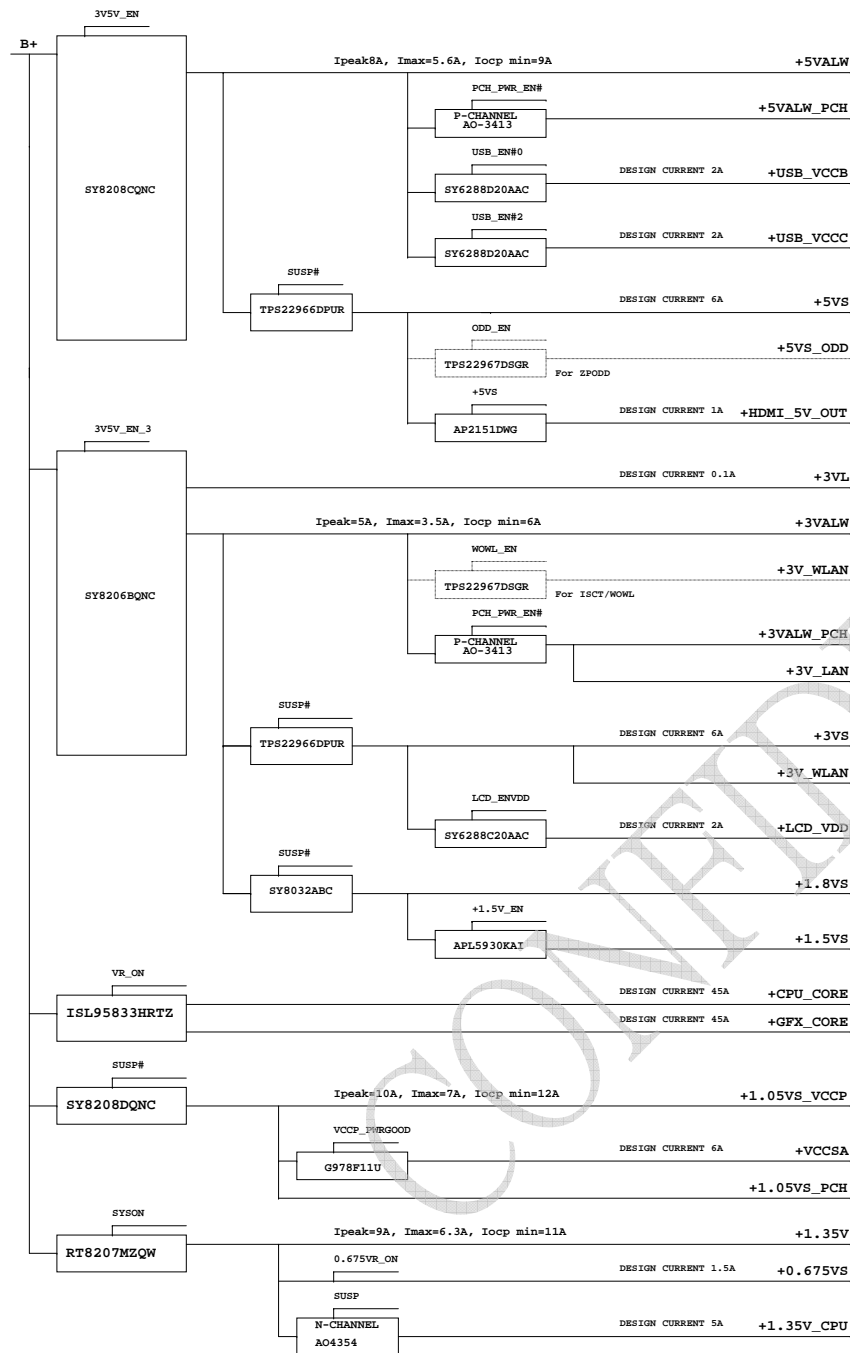
SATA HDD
SATA port 0
page 25

SATA Gen2 1x
5V 3GHz(300MB/s)

SATA ODD
SATA port 2
page 25

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| Compal Electronics, Inc. | | Block Diagram | |
|--------------------------|-----------------------------|---------------|---------|
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Voltage Rails

(O MEANS ON X MEANS OFF)

| power plane State | +RTCVCC | B+ +LCD_INV | +3VL | +5VALW +3VALW | +1.35V | +5VS +3VS +1.8VS +1.5VS +1.35V_CPU +0.675VS +CPU_CORE +GFX_CORE +VCCSA +1.05VS_VCCP +3V_WLAN +LCD_VDD |
|--------------------------------|---------|----------------|------|------------------|--------|--|
| S0 | O | O | O | O | O | O |
| S1 | O | O | O | O | O | O |
| S3 | O | O | O | O | O | X |
| S5 S4/AC | O | O | O | O | X | X |
| S5 S4/ Battery only | O | O | O | X | X | X |
| S5 S4/AC & Battery don't exist | O | X | X | X | X | X |

PCH SM Bus Address

| Power | Device | HEX | Address |
|-------|---------------|------|-------------|
| +3VS | DDR SO-DIMM 0 | A0 H | 1010 0000 b |
| +3VS | DDR SO-DIMM 1 | A4 H | 1010 0100 b |
| +3VS | Touch Pad | | |

EC SM Bus1 Address

| Power | Device | HEX | Address |
|-------|---------------|------|-------------|
| +3VL | Smart Battery | 16 H | 0001 0110 b |
| +3VL | Smart Charger | 12 H | 0001 0010 b |

EC SM Bus2 Address

| Power | Device | HEX | Address |
|-------|--------|------|-------------|
| +3VS | PCH | 96 H | 1001 0110 b |

BTO Option Table

| Function | CPU | PCH | ISPD | EMI/ESD/RF part | | | | |
|-------------|------------|---------------|-----------|-----------------|-------|------|-------|------|
| description | Ivy Bridge | Panther Point | HDMI LOGO | EMI/ESD/RF part | | | | |
| explain | i3-3217U | HM76 | HDMI LOGO | EMI/ESD/RF part | | | | |
| BTO | CPUR1@ | HM76R1@ | HDMI45@ | EMI@ | @EMI@ | ESD@ | @ESD@ | @RF@ |

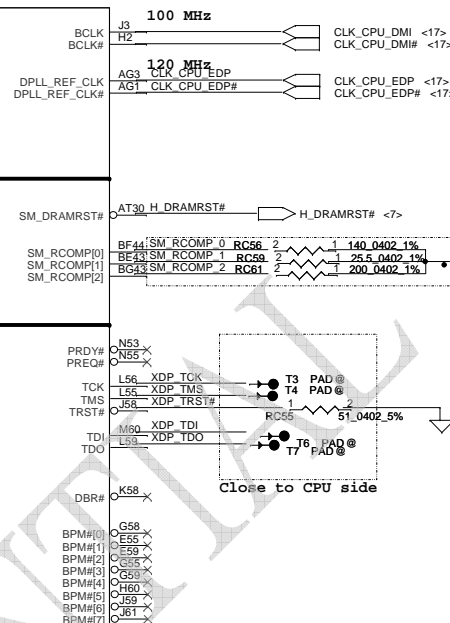
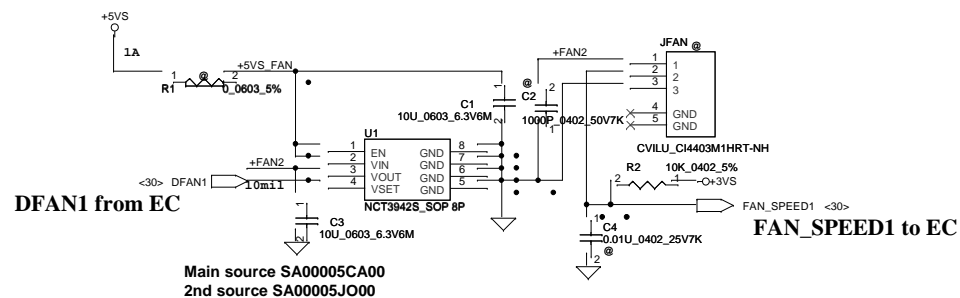
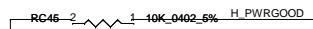
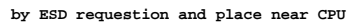
Red Word: always un-mount

| Function | LVDS-eDP | | Camera | CRT | | ISCT | |
|-------------|----------|-------|----------|--------|----------|--------|-------|
| description | LVDS-eDP | | Camera | CRT | | ISCT | |
| explain | LVDS | eDP | Camera | w/ CRT | w/o CRT | w/ | w/o |
| BTO | LVDS@ | IEDP@ | CAM_EMI@ | CRT@ | CRT@EMI@ | NOCRT@ | ISCT@ |

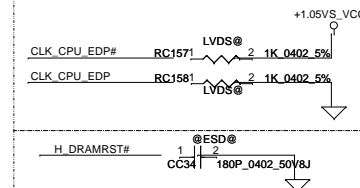
| Function | ZPODD | | TPM | Touch Screen | |
|-------------|--------|--------|---------|--------------|--|
| description | ZPODD | | TPM | Touch Screen | |
| explain | w/ | w/o | NPCT650 | w/ TOUCH | |
| BTO | ZPODD@ | NONZP@ | TPM@ | TOUCH_EMI@ | |

| STATE | SIGNAL | SLP_S3# | SLP_S4# | SLP_S5# |
|----------------------|--------|---------|---------|---------|
| Full ON | | HIGH | HIGH | HIGH |
| S1(Power On Suspend) | | HIGH | HIGH | HIGH |
| S3 (Suspend to RAM) | | LOW | HIGH | HIGH |
| S4 (Suspend to Disk) | | LOW | LOW | HIGH |
| S5 (Soft OFF) | | LOW | LOW | LOW |
| G3 | | LOW | LOW | LOW |

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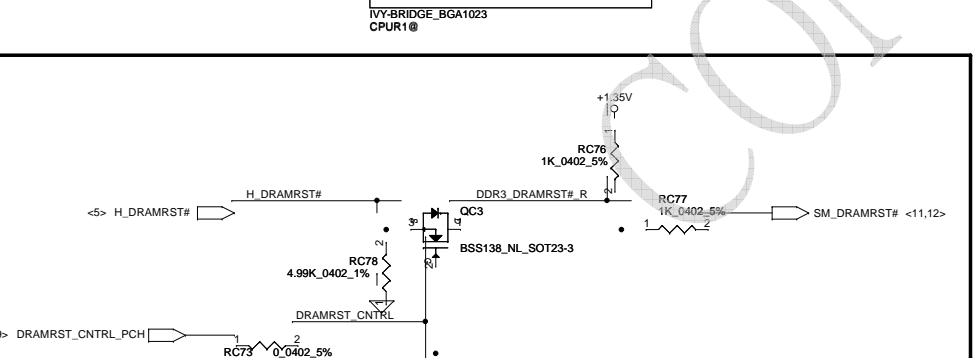
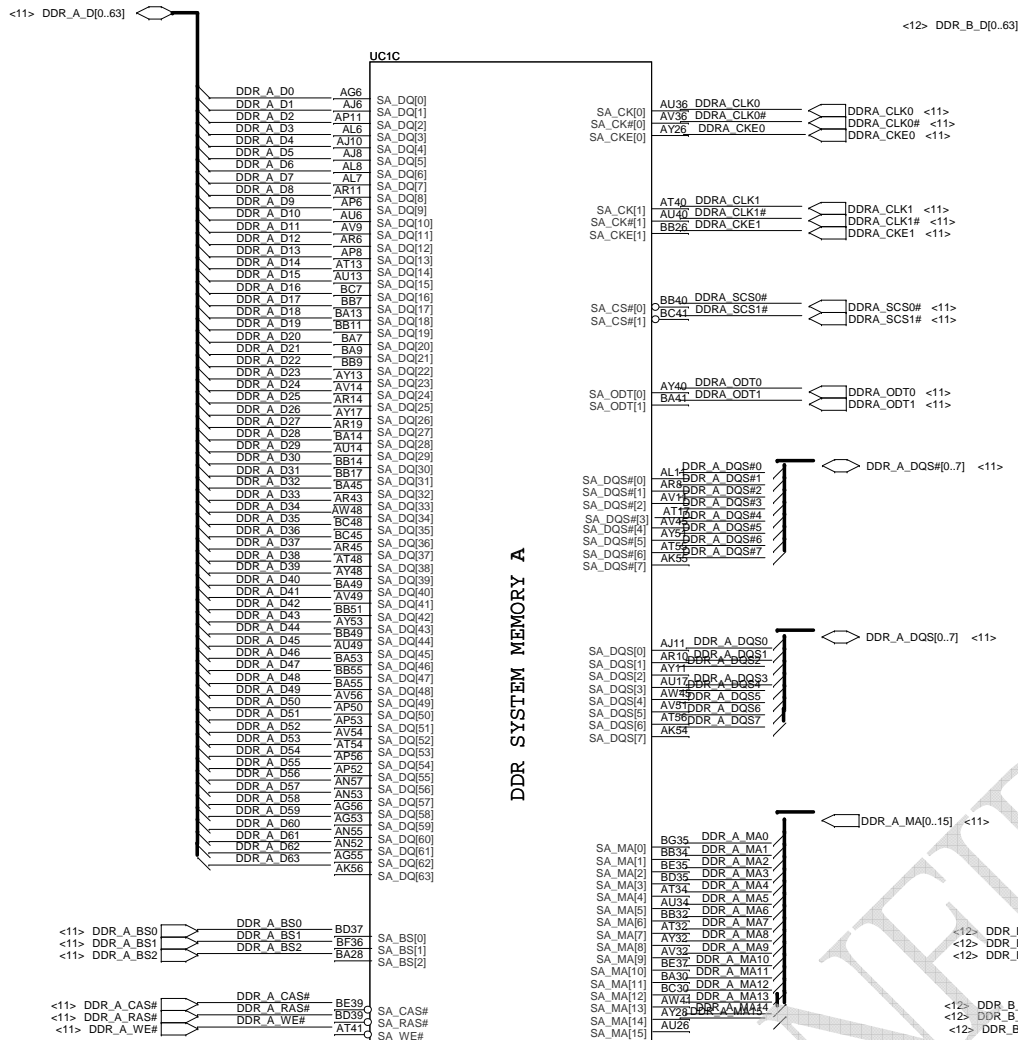
Stuff RC158&RC157 if do not support eDP



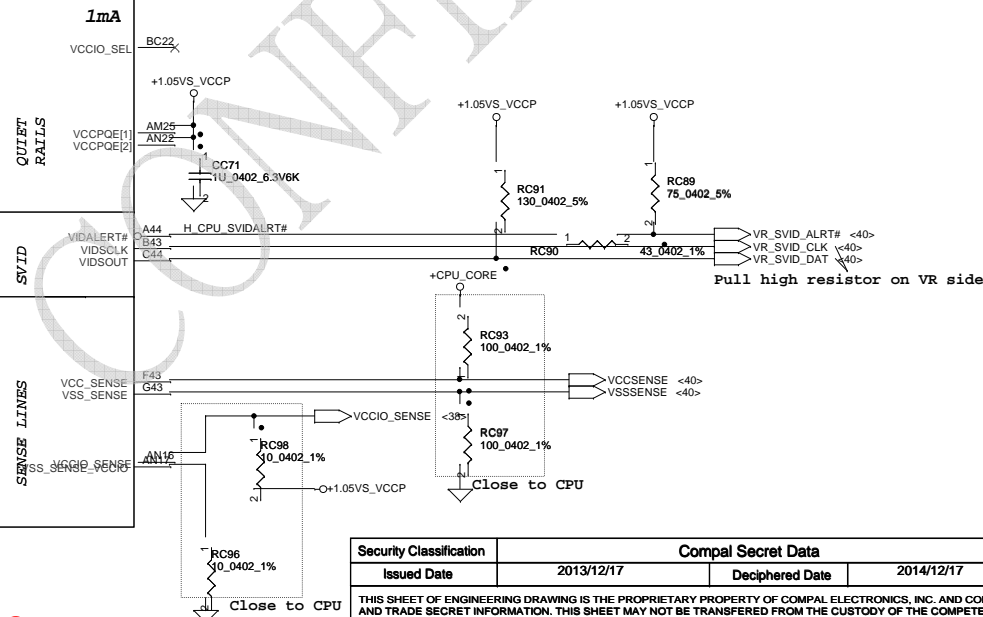
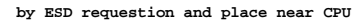
by ESD requestion and place near CPU

DDR3 Compensation Signals
Layout Note: Place these
resistors near Processor

| | | | | | |
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POWER

+GFX_CORE
UC1G
29A

AA46 VAXG[1]
AB47 VAXG[2]
AB50 VAXG[3]
AB51 VAXG[4]
AB52 VAXG[5]
AB53 VAXG[6]
AB55 VAXG[7]
AB56 VAXG[8]
AB58 VAXG[9]
AB59 VAXG[10]
AC61 VAXG[11]
AD47 VAXG[12]
AD48 VAXG[13]
AD50 VAXG[14]
AD51 VAXG[15]
AD52 VAXG[16]
AD53 VAXG[17]
AD55 VAXG[18]
AD56 VAXG[19]
AD58 VAXG[20]
AE46 VAXG[21]
N45 VAXG[22]
P47 VAXG[23]
P48 VAXG[24]
P50 VAXG[25]
P51 VAXG[26]
P52 VAXG[27]
P53 VAXG[28]
P55 VAXG[29]
P56 VAXG[30]
P58 VAXG[31]
P61 VAXG[32]
T48 VAXG[33]
T58 VAXG[34]
T59 VAXG[35]
T61 VAXG[36]
U46 VAXG[37]
V47 VAXG[38]
V48 VAXG[39]
V50 VAXG[40]
V51 VAXG[41]
V52 VAXG[42]
V53 VAXG[43]
V55 VAXG[44]
V56 VAXG[45]
V58 VAXG[46]
W50 VAXG[47]
W51 VAXG[48]
W52 VAXG[49]
W53 VAXG[50]
W55 VAXG[51]
W56 VAXG[52]
W61 VAXG[53]
V48 VAXG[54]
V50 VAXG[55]
V51 VAXG[56]

GRAPHICS

DDR3 - 1.5V RAILS

1mA

QUIET RAILS

SENSE LINES

SA RAIL

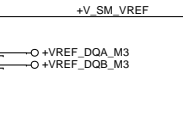
VCCSA_VID

11ms

IVY-BRIDGE_BGA1023

CPU1@

+V_SM_VREF should have 20 mil trace width



Place TOP IN BGA

Place BOT OUT BGA

Place TOP IN BGA

Place BOT OUT BGA

Place TOP IN BGA

Place BOT OUT BGA

Place TOP IN BGA

Place BOT OUT BGA

Place TOP IN BGA

Place BOT OUT BGA

Place TOP IN BGA

Place BOT OUT BGA

Place TOP IN BGA

Place BOT OUT BGA

Place TOP IN BGA

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Place BOT OUT BGA

Place TOP IN BGA

Place BOT OUT BGA

Place TOP IN BGA

Place BOT OUT BGA

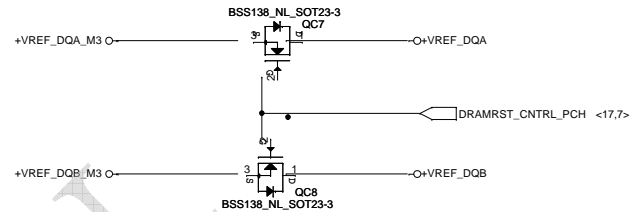
Place TOP IN BGA

Place BOT OUT BGA

Place TOP IN BGA

Place BOT OUT BGA

Intel DDR Vref M3

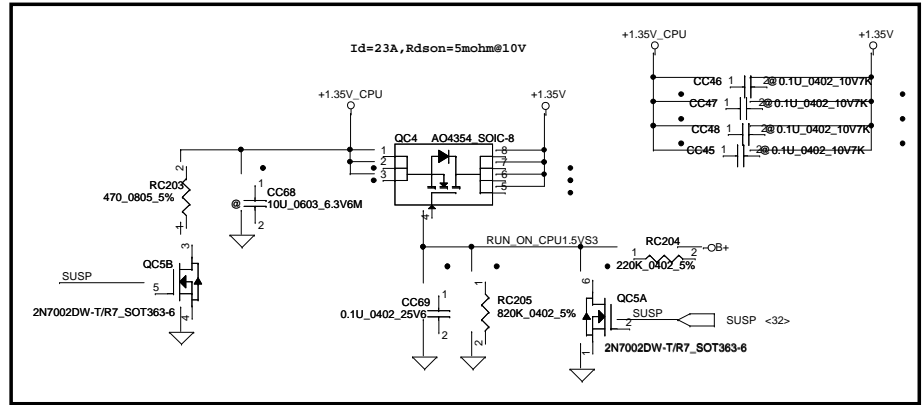
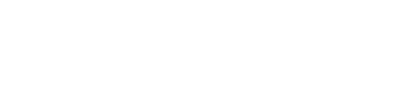
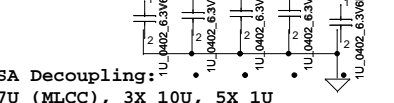
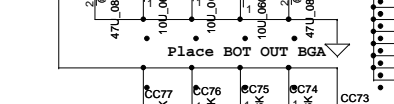
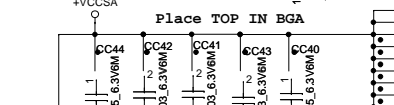
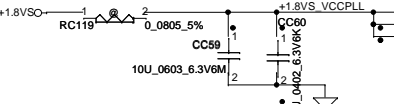


+1.35V_CPU Decoupling:
2X 47U(MLCC), 6X 10U, 8X 1U

| VCCSA_VID0 | VCCSA_VID1 | +VCCSA |
|------------|------------|---------|
| 0 | 0 | 0.90 V |
| 0 | 1 | 0.80 V |
| 1 | 0 | 0.725 V |
| 1 | 1 | 0.675 V |

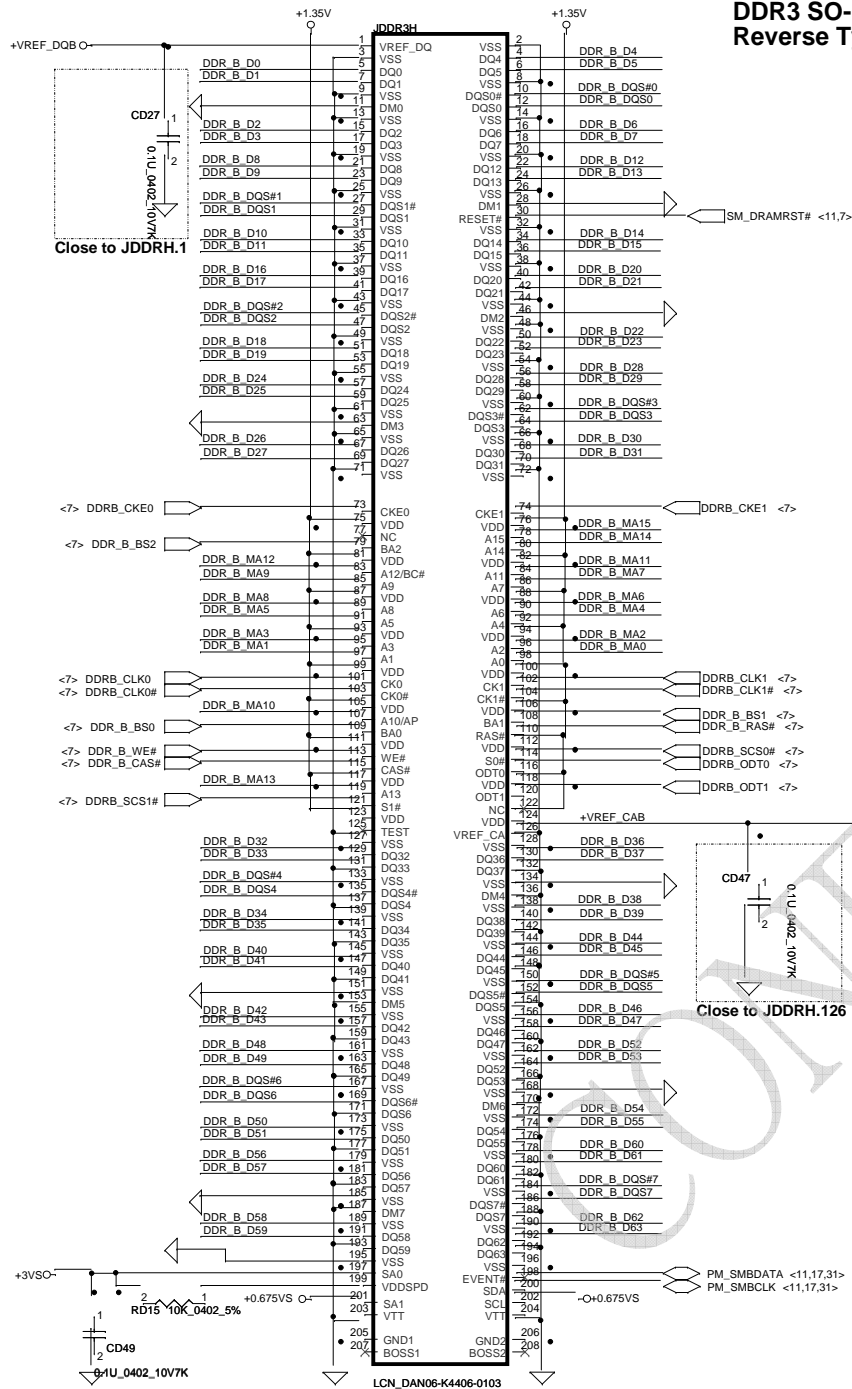
For Sandy Bridge

VCCPLL Decoupling:
1X 330U (6m ohm), 1X 10U, 2X 1U

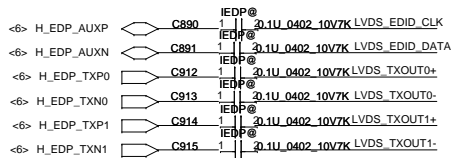




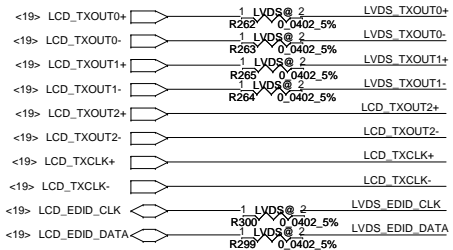
DDR3 SO-DIMM B Reverse Type



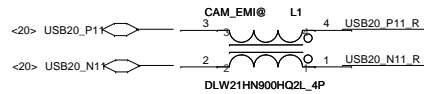
For eDP Panel



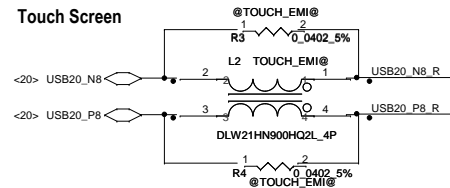
For LVDS 1ch Panel



Camera

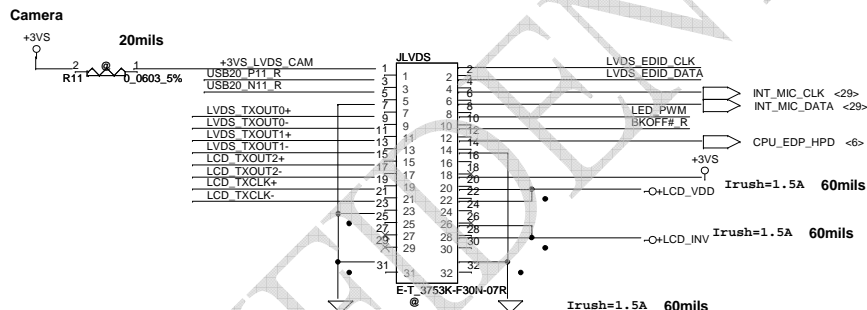


Touch Screen



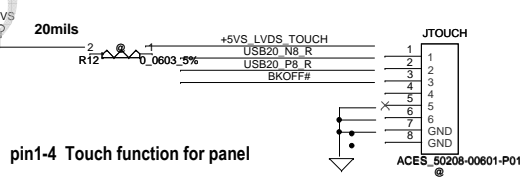
Reserve for EMI request

LVDS colay eDP cable



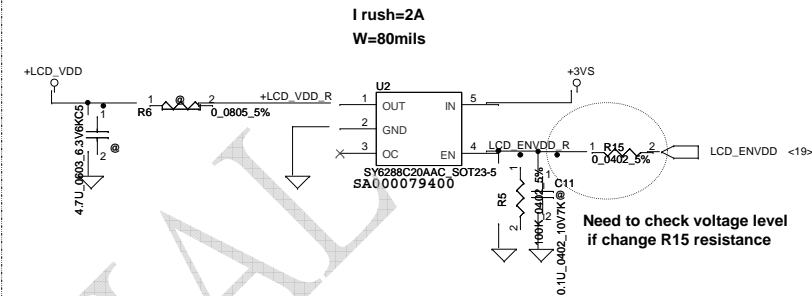
pin1,3,5,6,7,8 Camera function with single or dual MIC
pin2,4,9,10-30 For LVDS or EDP panel

Touch Screen

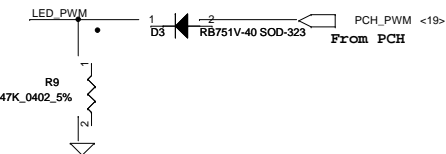
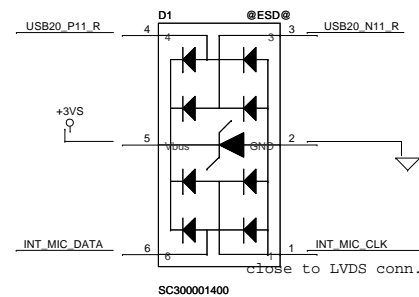


pin1-4 Touch function for panel

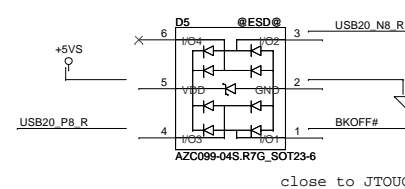
LCD POWER CIRCUIT



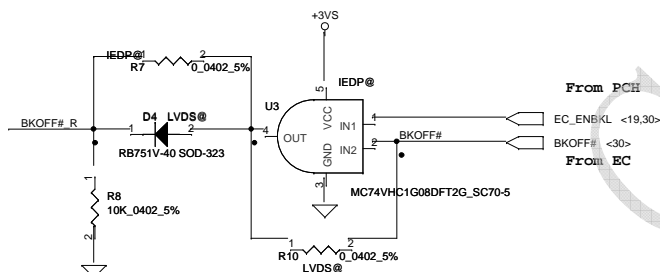
Camera & MIC



Touch Panel

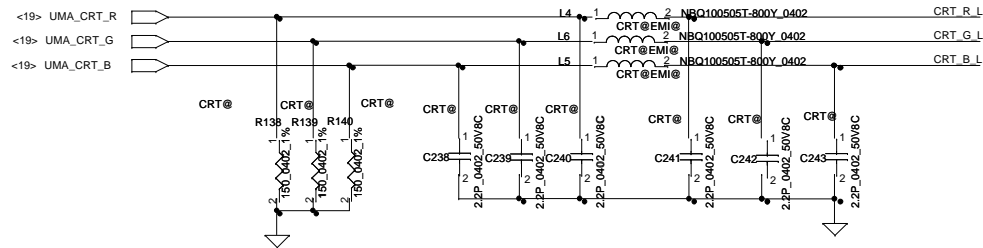


Reserve for eDP panel potential issue

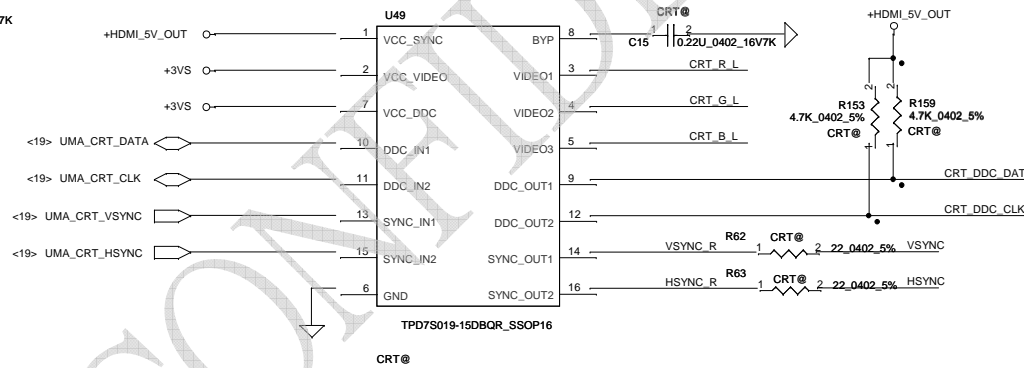
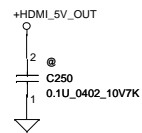
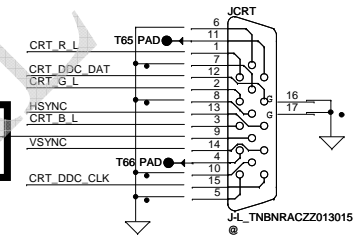


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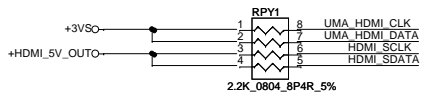
CRT CONNECTOR



USE HDMI POWER



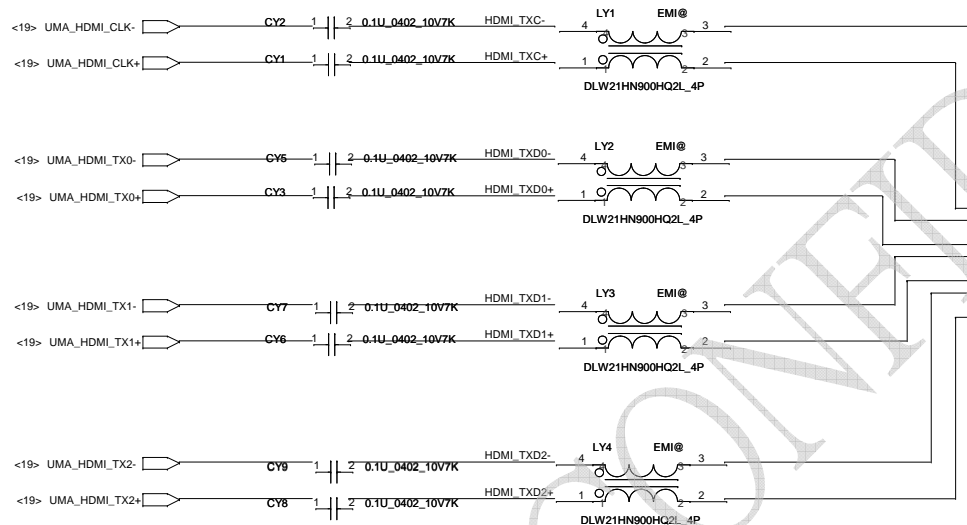
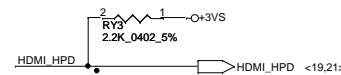
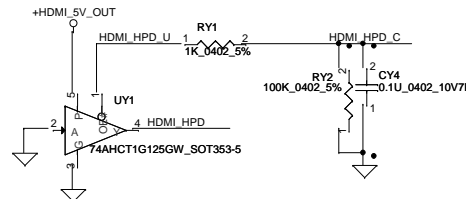
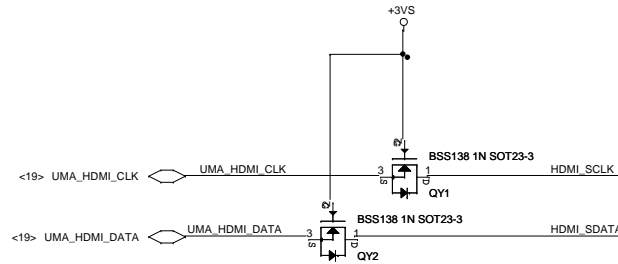
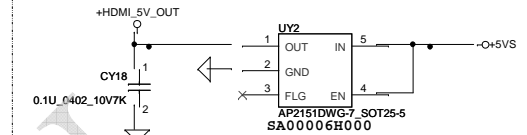
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| Security Classification | Compal Secret Data | | | Compal Electronics, Inc. | | |
| Issued Date | 2013/12/17 | Deciphered Date | 2014/12/17 | Title | | |
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| | | | | Date | Wednesday, January 22, 2014 | Sheet 14 of 41 |



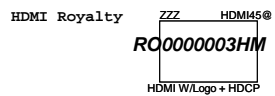
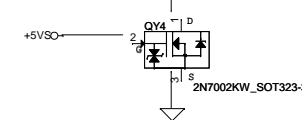
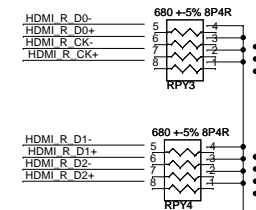
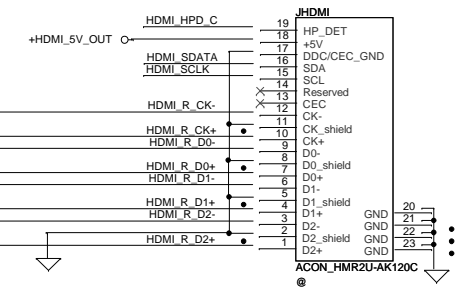
| OE# | A | Y |
|-----|---|---|
| L | L | L |
| L | H | H |
| H | X | Z |

HDMI POWER CIRCUIT

VIN = 5V, IOUT = 0.5A, RDS(ON) TYP=95m ; MAX=115m
Current Limit: TYP=0.8A ; MAX=1A

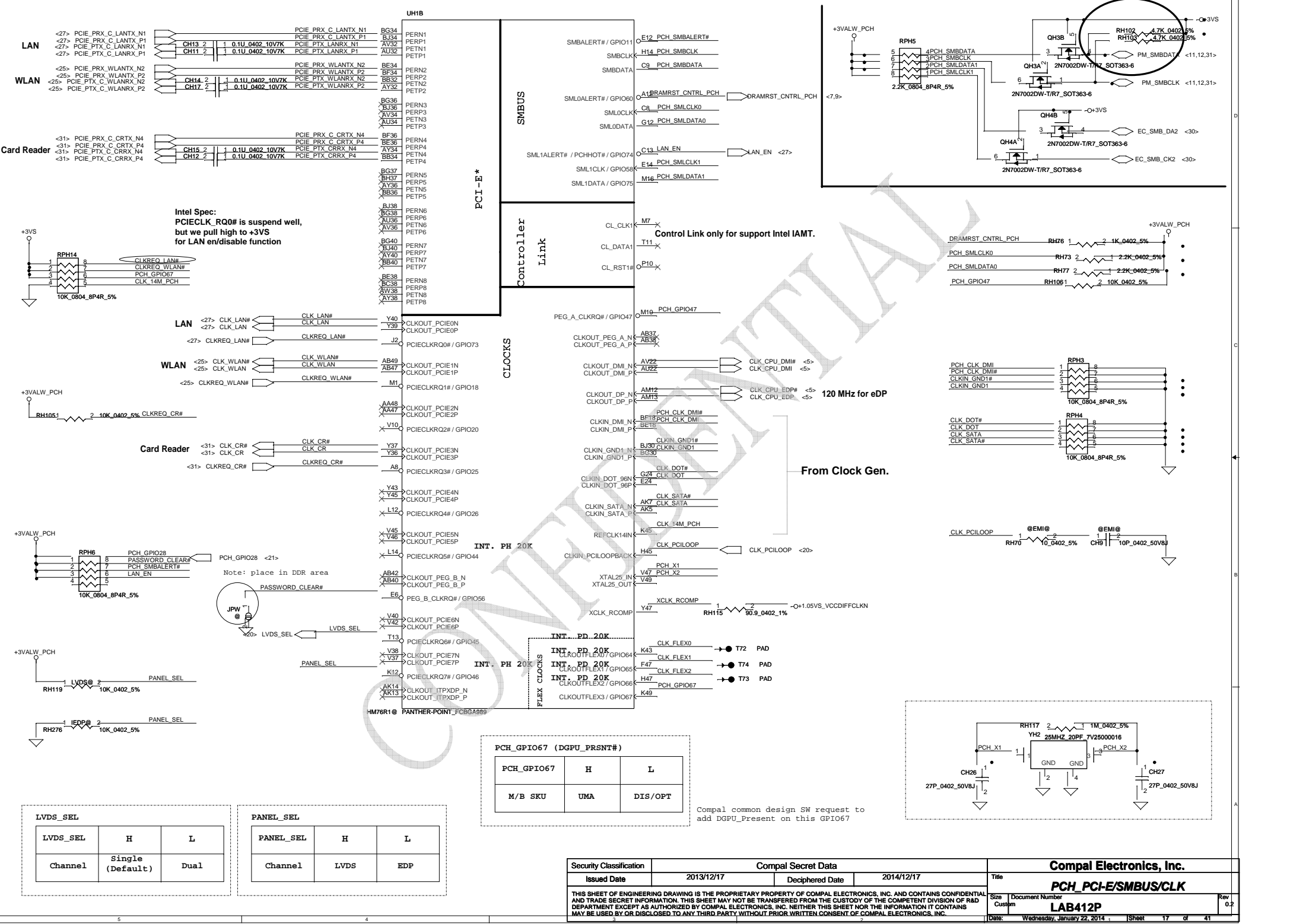


HDMI Connector



HDMI W/O Logo: R00000001HM
HDMI W/Logo: R00000002HM
HDMI W/Logo + HDCP: R00000003HM
please manually load
this virtual material to 45@ BOM

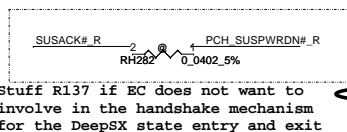
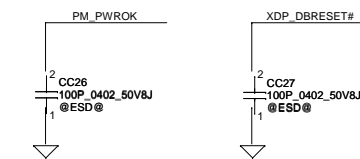
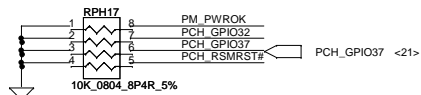
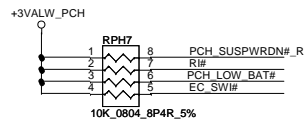
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| | | | | Date | Wednesday, January 22, 2014 |
| | | | | Sheet | 15 of 41 |



| | | | | | |
|----------|------------------|------|-----------|------|-----|
| LVDS_SEL | | | PANEL_SEL | | |
| LVDS_SEL | H | L | PANEL_SEL | H | L |
| Channel | Single (Default) | Dual | Channel | LVDS | EDP |

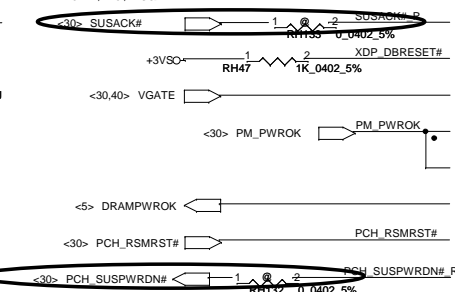
| | | |
|---------------------------|-----|---------|
| PCH_GPIO67 (DGPU_PRSENT#) | | |
| PCH_GPIO67 | H | L |
| M/B SKU | UMA | DIS/OPT |

| | | | | | |
|----------|------------------|------|-----------|------|-----|
| LVDS_SEL | | | PANEL_SEL | | |
| LVDS_SEL | H | L | PANEL_SEL | H | L |
| Channel | Single (Default) | Dual | Channel | LVDS | EDP |



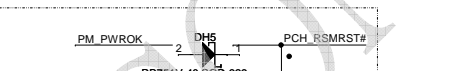
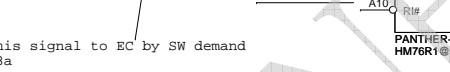
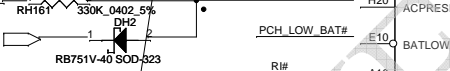
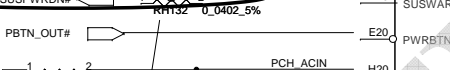
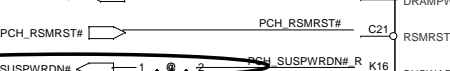
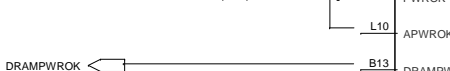
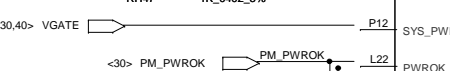
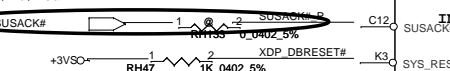
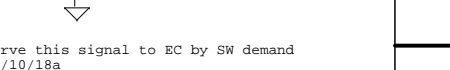
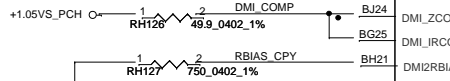
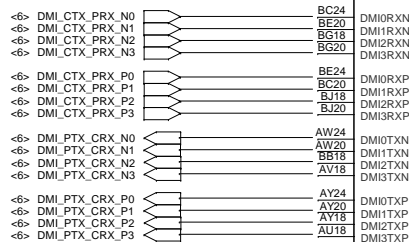
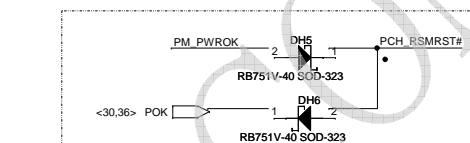
Stuff R137 if EC does not want to involve in the handshake mechanism for the DeepSX state entry and exit

Reserve this signal to EC by SW demand 2011/10/18a



Reserve this signal to EC by SW demand 2011/10/18a

Reserve this signal to EC by SW demand 2011/10/18a



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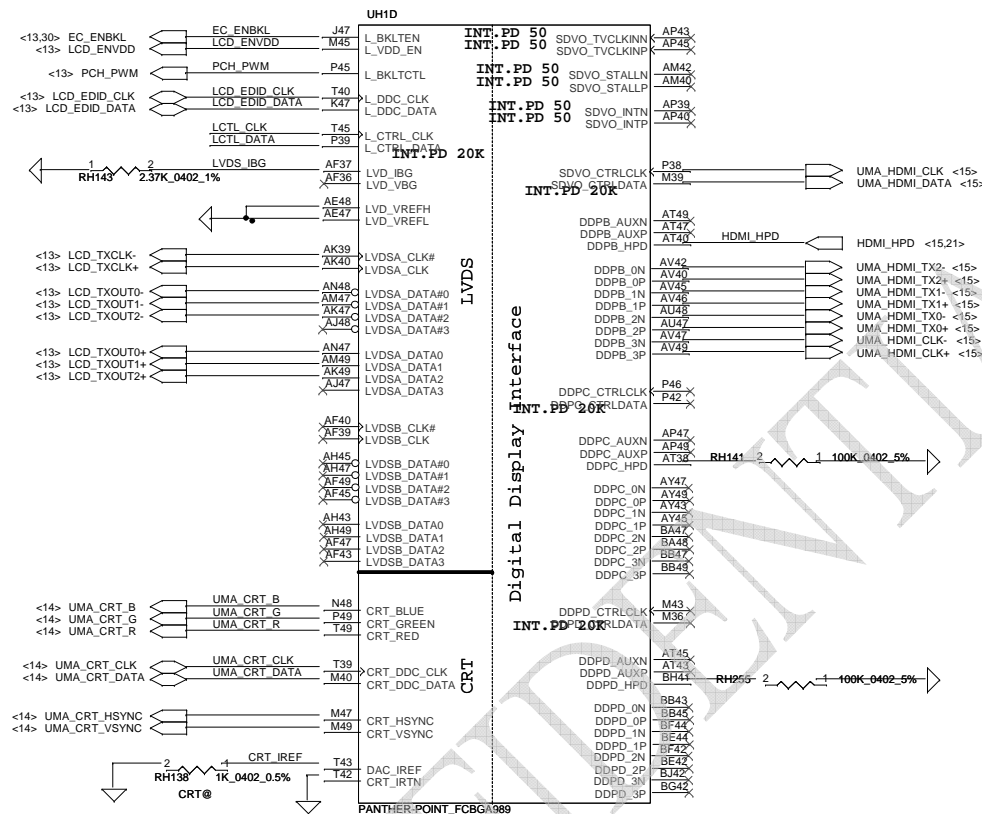
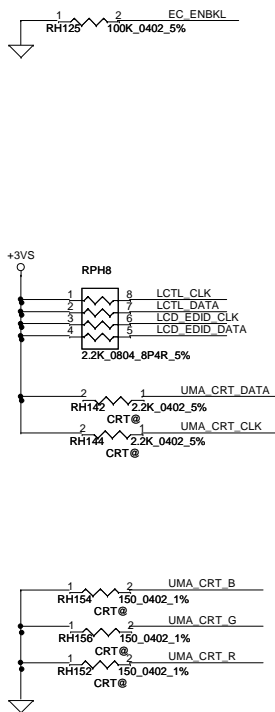
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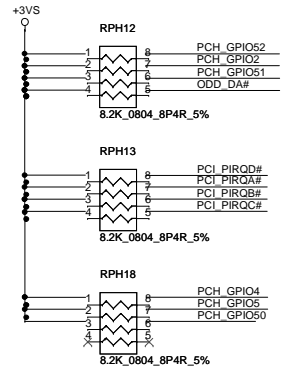
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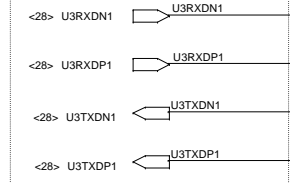


RH138
1K_0402_5%
NOCRT@

| | | | | |
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| | | | | Rev 0.2 |
| | | | | Date: Wednesday, January 22, 2014 |
| | | | | Sheet 19 of 41 |



USB-Right Front (USB3.0 port)



<21> PCH_GPIO54

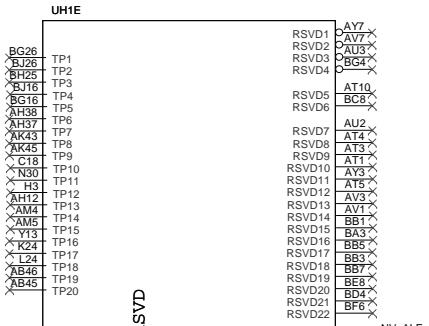
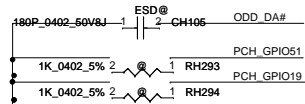
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<25,26,27,30,31,5> PLT_RST#

<30> CLK_PCI_EC

<17> CLK_PCILoop

<26> CLK_PCI_TPM_R



RSVD

INT.PD 20K

EHCI 1

EHCI 2

PCI

INT.PD 20K

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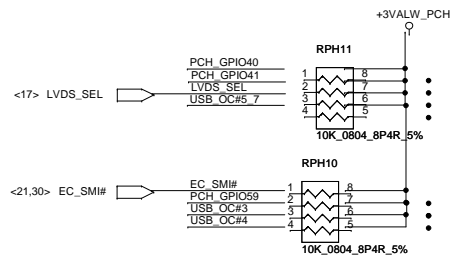
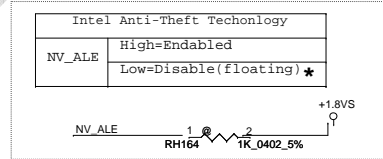
| Boot BIOS Strap | | |
|-----------------|------------|--------------------|
| PCH_GPIO51 | PCH_GPIO19 | Boot BIOS Location |
| 0 | 0 | LPC |
| 0 | 1 | Reserved |
| 1 | 0 | PCI |
| 1 | 1 | SPI * |

| A16 Swap Override Strap | |
|-------------------------|---------------------------------|
| WL_OFF# | |
| * | Low= A16 swap override Enable |
| | High= A16 swap override Disable |

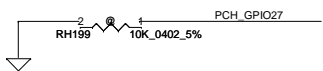
USB-Right Front
USB-Right Rear
USB-Left

Touch Screen
WiMax/BT

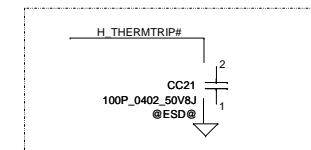
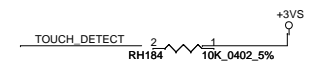
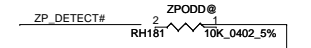
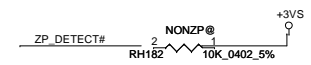
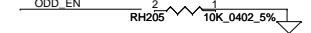
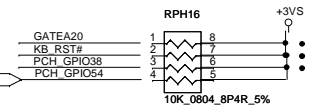
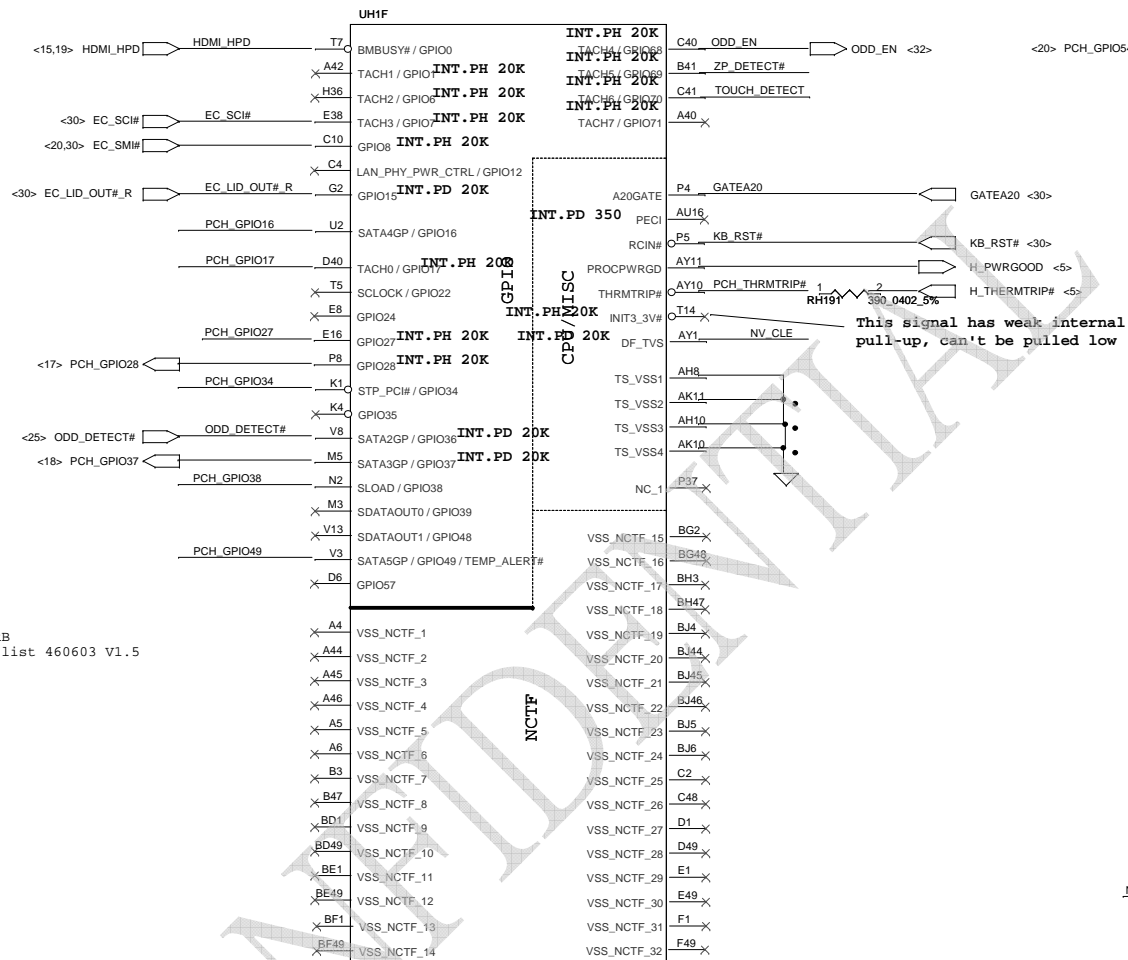
Int. Camera



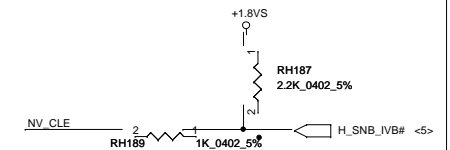
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| | | | | Rev | 0.2 |
| | | | | Date | Wednesday, January 22, 2014 |
| | | | | Sheet | 20 of 41 |



Follow Compal ORB
and Intel Check list 460603 V1.5



| | |
|-------------------------------|----------------------|
| DMI & FDI Termination Voltage | |
| NV_CLE | Set to VCC when HIGH |
| | Set to VSS when LOW |

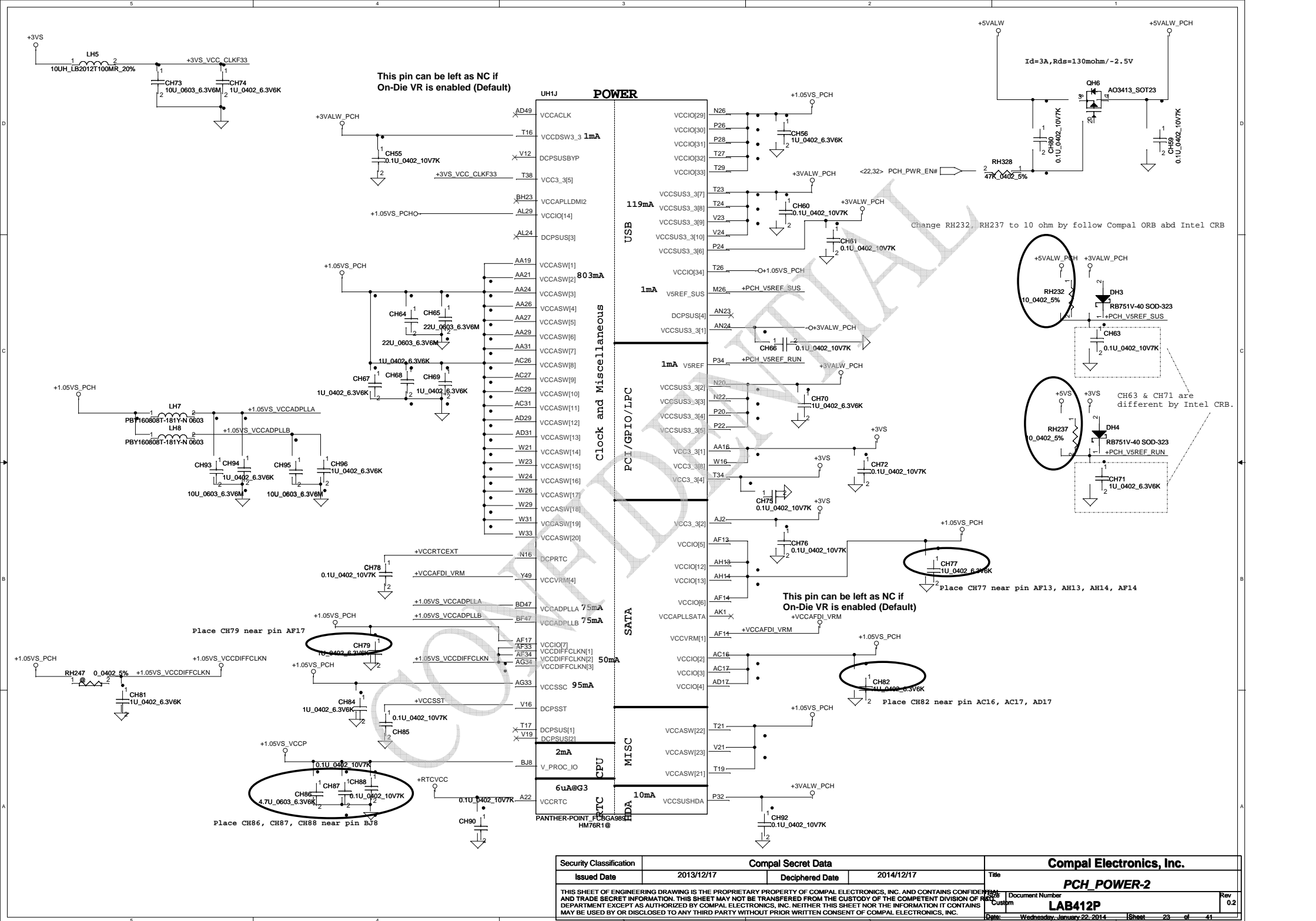


```
GPIO28 (pull high on P.17)
On-Die PLL Voltage Regulator
* H: Enable
  L: Disable
```

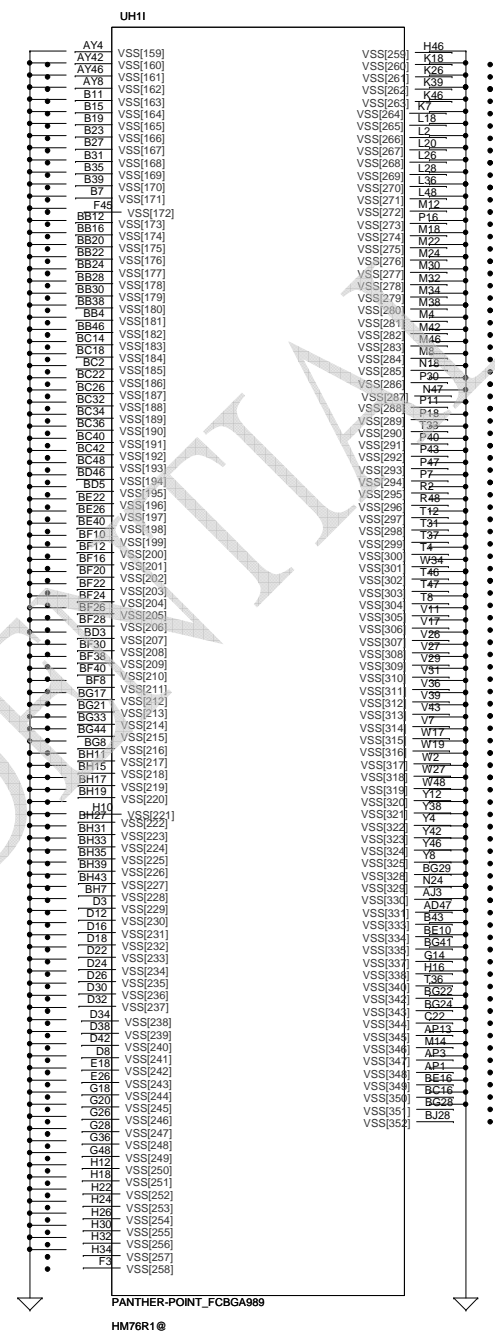
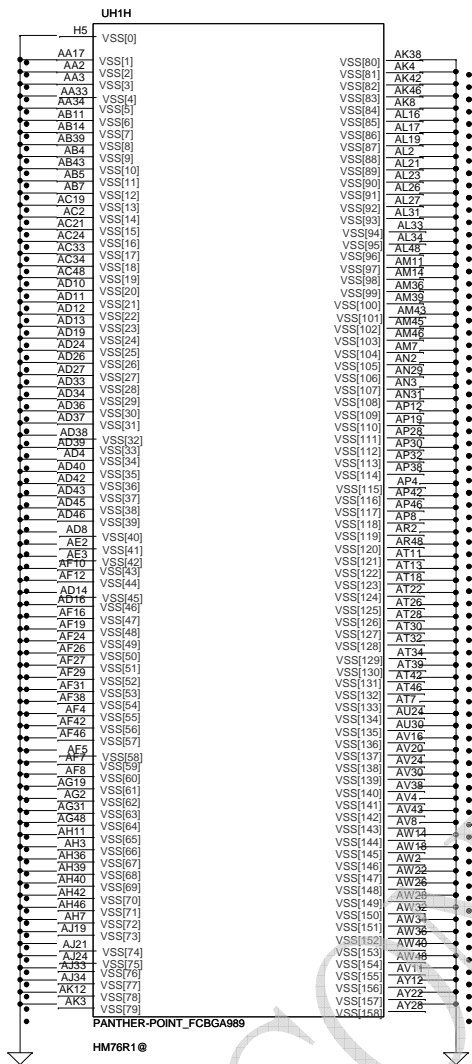
```
GPIO8
Integrated Clock Chip Enable (Removed)
H: Disable
* L: Enable
```

Integrated clock enable functionality
is achieved by soft-strap
The current default is clock enable

| OPTIMUS_EN# | | |
|-------------|--------|---------|
| OPTIMUS_EN# | H | L |
| SKU | NonOPT | Optimus |

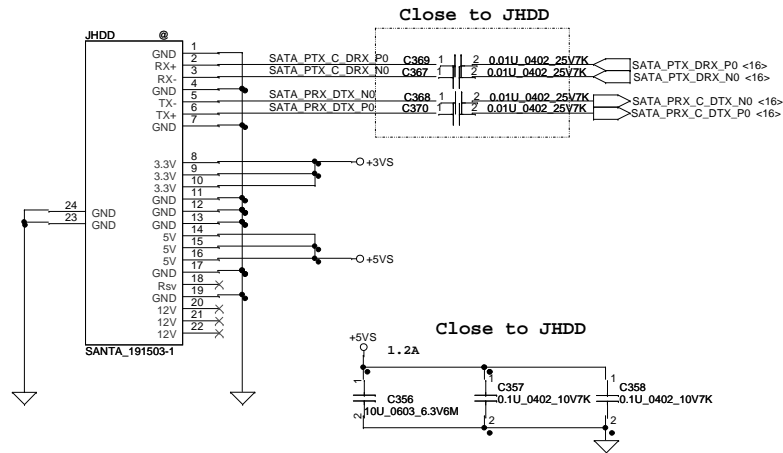


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| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
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| | | | | Customer | LAB412P |
| Date: | | | | Wednesday, January 22, 2014 | Sheet 23 of 41 |

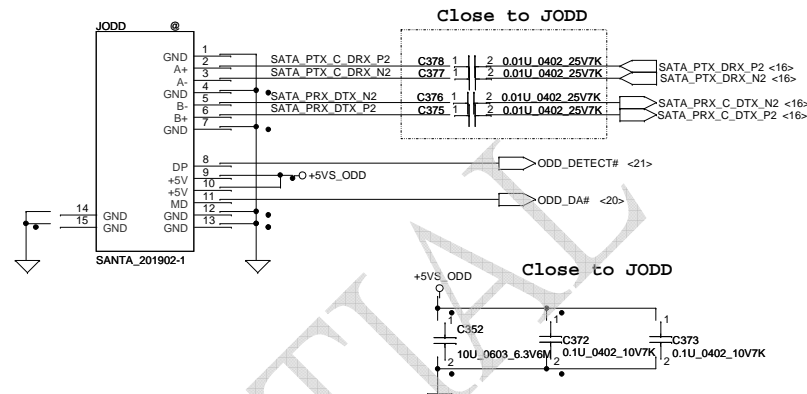


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|---|------------|-----------------------------|------------|--------------------------|----------|
| Security Classification | | Compal Secret Data | | Compal Electronics, Inc. | |
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| | | | | PCH_GND | |
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| | | | | LAB412P | 0.2 |
| Date | | Wednesday, January 22, 2014 | | Sheet | 24 of 41 |

SATA HDD Conn.



SATA ODD Conn



| Power Consumption | |
|-------------------|---------|
| Peak | 1800 mA |
| Read (CD) | 1100 mA |
| Read (DVD) | 950 mA |
| Write | 1300 mA |
| Standby | 20mA |

NGFF-Slot1-E-Key-WLAN

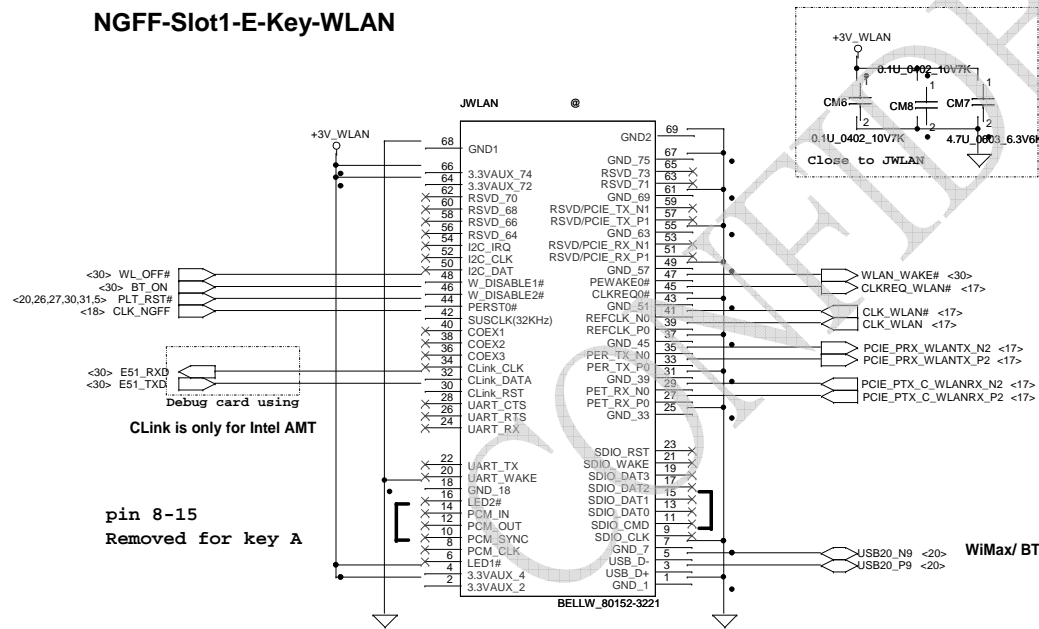
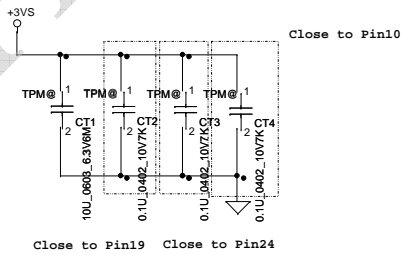
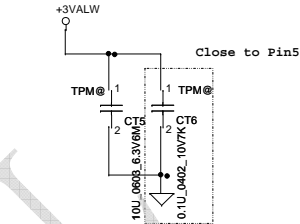
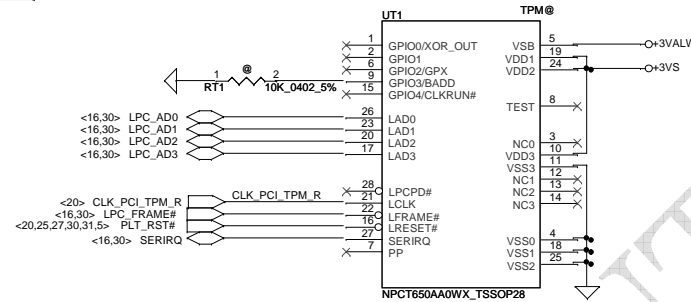
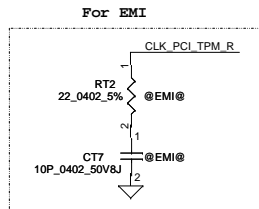


Table 23. SDIO Based Module Solution Pinout (Module Key E)

| Pin | Signal | Pin | Signal |
|-----|---------------------------------|-----|----------------------|
| 74 | RESERVED/REFCLKN1 | 75 | RESERVED/REFCLKP1 |
| 72 | RESERVED/REFCLKN1 | 73 | RESERVED/REFCLKP1 |
| 70 | UM_Power_In/GPIO/PWAKE1B | 71 | RESERVED/REFCLKP1 |
| 68 | UM_Power_Out/CURREQ1B | 69 | RESERVED/REFCLKP1 |
| 66 | UM_WSP/PERST1P | 67 | RESERVED/PERST1P |
| 64 | RESERVED | 65 | RESERVED/PERST1P |
| 62 | ALERT# (IO#2/3.3V) | 63 | RESERVED/PERST1P |
| 60 | IO#2 (IO#2/3.3V) | 61 | RESERVED/PERST1P |
| 58 | IO#2 (IO#2/3.3V) | 59 | RESERVED/PERST1P |
| 56 | W_DISABLE1 (IO#1/3.3V) | 57 | RESERVED/PERST1P |
| 54 | Reserved/W_DISABLE2 (IO#1/3.3V) | 55 | PWAKE1B (IO#1/3.3V) |
| 52 | PERST1P (IO#1/3.3V) | 53 | CLKREQ1B (IO#1/3.3V) |
| 50 | IO#2 (IO#2/3.3V) | 51 | RESERVED |
| 48 | IO#2 (IO#2/3.3V) | 49 | RESERVED |
| 46 | IO#2 (IO#2/3.3V) | 47 | RESERVED |
| 44 | IO#2 (IO#2/3.3V) | 45 | RESERVED |
| 42 | VENDOR DEFINED | 43 | RESERVED |
| 40 | VENDOR DEFINED | 41 | RESERVED |
| 38 | VENDOR DEFINED | 39 | RESERVED |
| 36 | IO#2 (IO#2/3.3V) | 37 | RESERVED |
| 34 | IO#2 (IO#2/3.3V) | 35 | RESERVED |
| 32 | IO#2 (IO#2/3.3V) | 33 | RESERVED |
| 30 | IO#2 (IO#2/3.3V) | 31 | RESERVED |
| 28 | IO#2 (IO#2/3.3V) | 29 | RESERVED |
| 26 | IO#2 (IO#2/3.3V) | 27 | RESERVED |
| 24 | IO#2 (IO#2/3.3V) | 25 | RESERVED |
| 22 | IO#2 (IO#2/3.3V) | 23 | RESERVED |
| 20 | IO#2 (IO#2/3.3V) | 21 | RESERVED |
| 18 | IO#2 (IO#2/3.3V) | 19 | RESERVED |
| 16 | IO#2 (IO#2/3.3V) | 17 | RESERVED |
| 14 | IO#2 (IO#2/3.3V) | 15 | RESERVED |
| 12 | IO#2 (IO#2/3.3V) | 13 | RESERVED |
| 10 | IO#2 (IO#2/3.3V) | 11 | RESERVED |
| 8 | IO#2 (IO#2/3.3V) | 9 | RESERVED |
| 6 | IO#2 (IO#2/3.3V) | 7 | RESERVED |
| 4 | IO#2 (IO#2/3.3V) | 5 | RESERVED |
| 2 | IO#2 (IO#2/3.3V) | 3 | RESERVED |

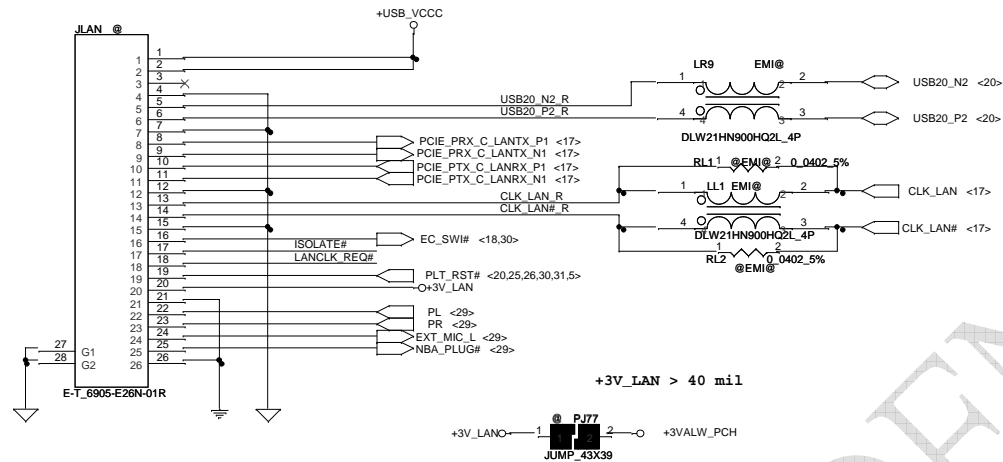
TPM

| BADD | ADDRESS |
|------------|-----------|
| 0 | EEh - EFh |
| * Floating | 7Eh - 7Fh |



| | | | | |
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| | | | | Sheet 26 of 41 |

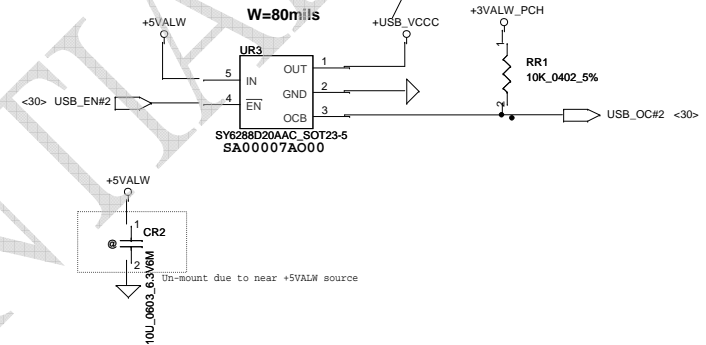
LAN/USB Small board Conn



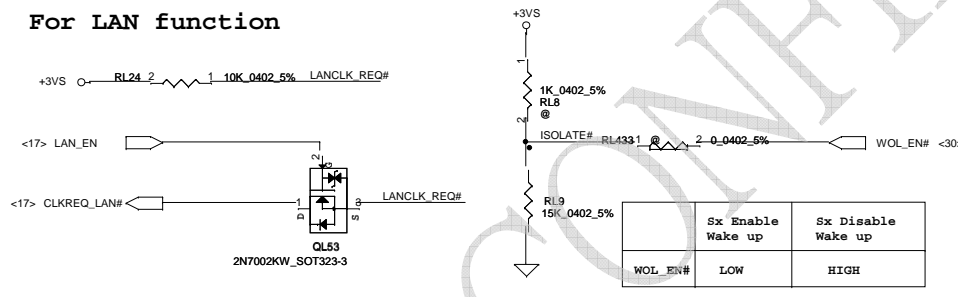
Left USB 2.0 x 1

Current Limit 2A

Check Output, Caps are on sub-board or not.



For LAN function



| LAN | WOL | LAN_EN | | ISOLATEB | |
|-----|-----|--------|----|----------|----|
| | | S0 | Sx | S0 | Sx |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 1 | 1 | 0* |

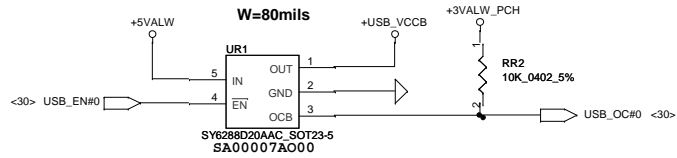
*
S3: after SUSP# assert low over 100ms
S4/S5: after SYSON assert low over 100ms

+3V_LAN rising time (10%~90%) need > 1ms and <100ms.

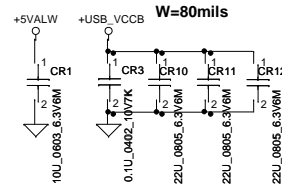
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|--|--|-----------------------------|-----------------|--------------------------|------------|------------|
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| LUSB20/LAN conn. | | | | | | Rev 0.2 |
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Right USB power switch

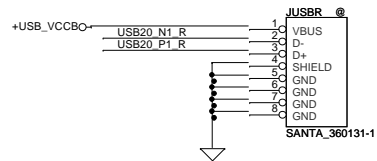
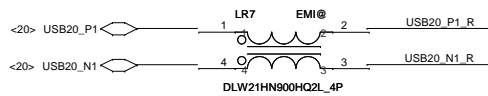
Current Limit 2A



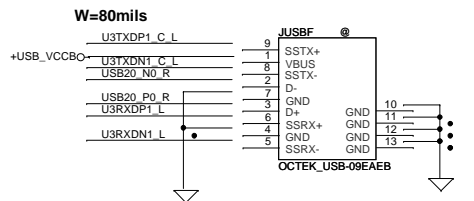
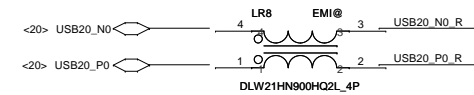
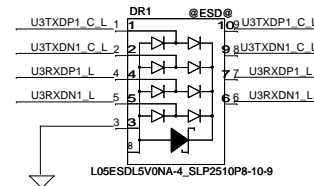
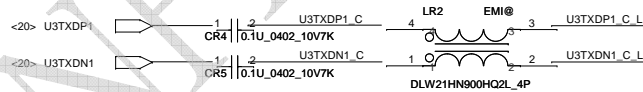
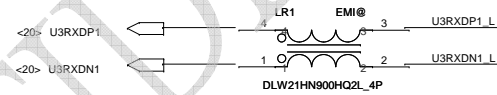
CLOSE to UR1



Right rear USB2.0 Conn.



Right front USB 3.0 Conn.

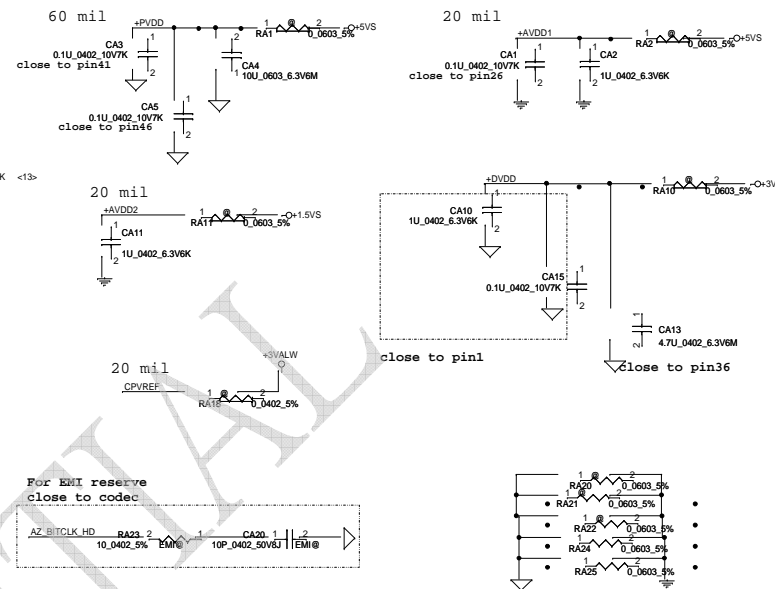


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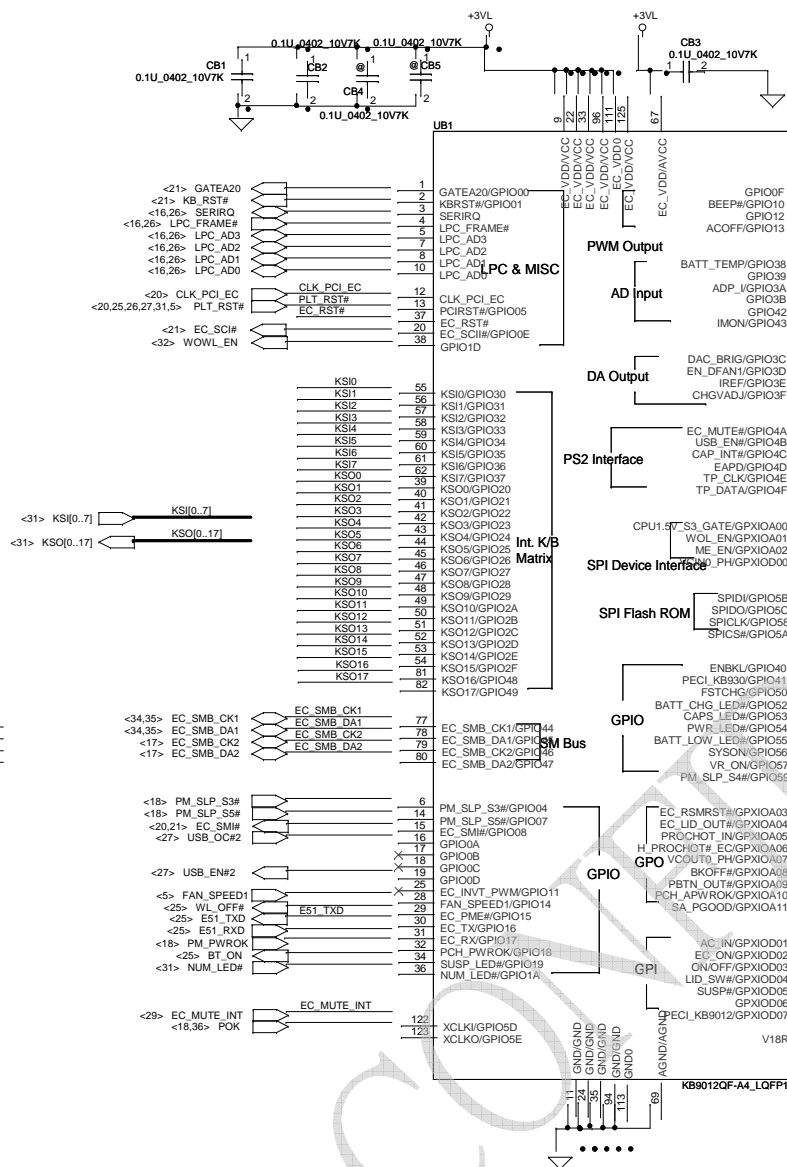
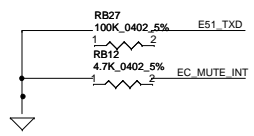
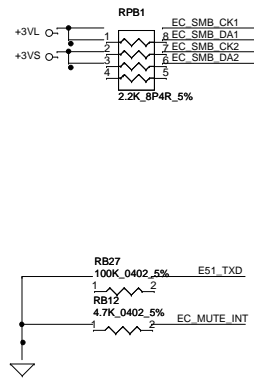
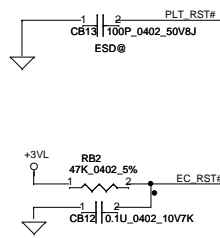
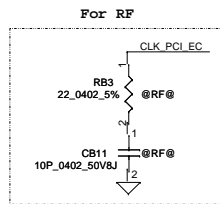
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RUSB20/30

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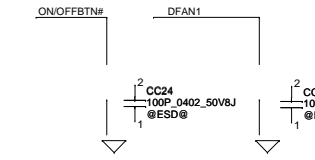
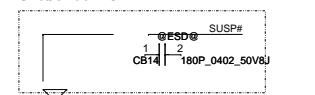
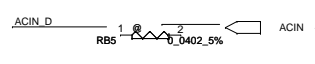
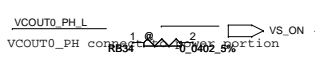
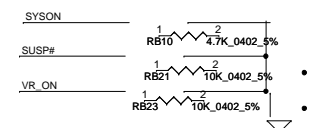
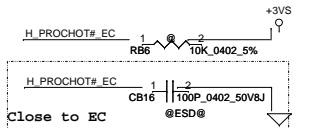
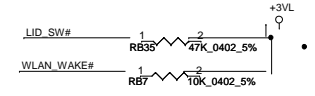
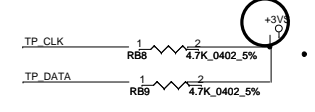
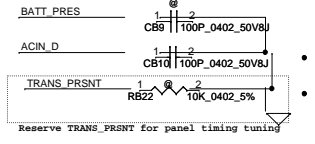
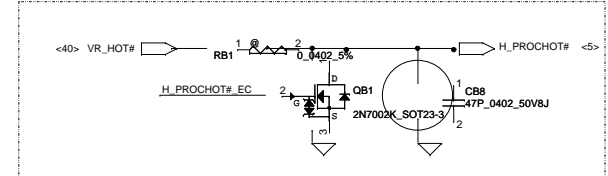


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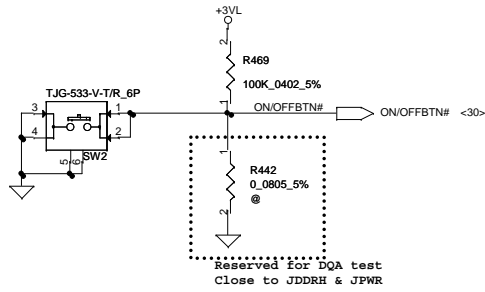


Voltage Comparator Pins FOR 9012 A4

| | | |
|---------------|----------------|---------------|
| VCIN0 pin109 | >1.2V | <1.2V |
| VCIN1 pin102 | HIGH (default) | LOW |
| VCOUT0 pin104 | HIGH (default) | LOW |
| VCOUT1 pin103 | HIGH | LOW (default) |

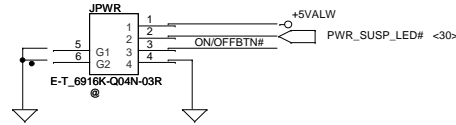


Power Button

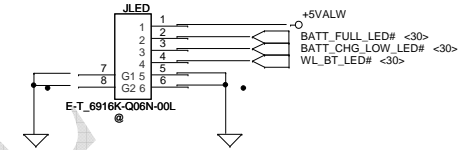


PBTN/B to M/B

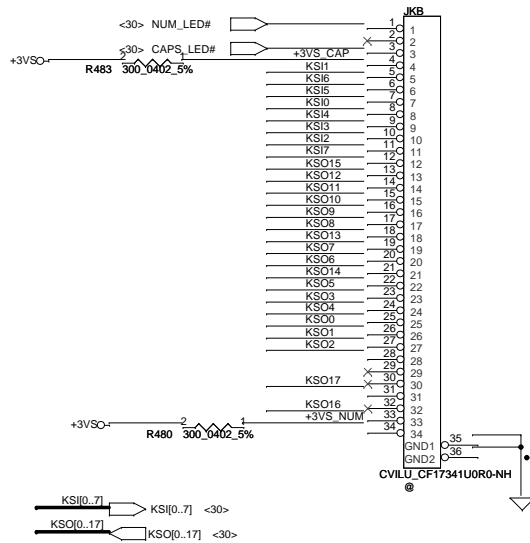
NOTICE: ON/OFFBTN# must have pull-high resistor on motherboard



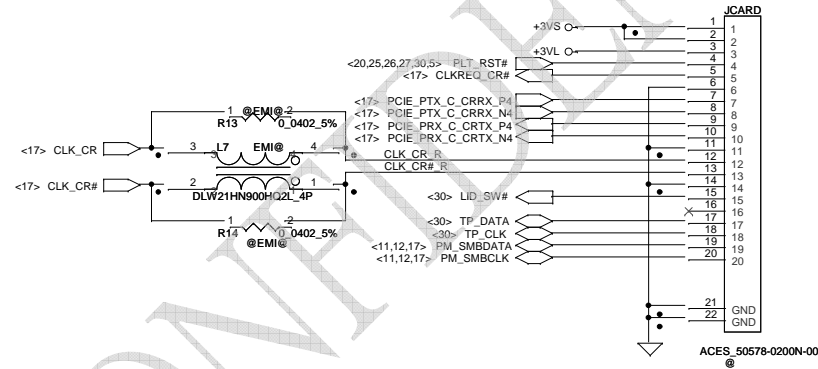
LED Small board to Conn



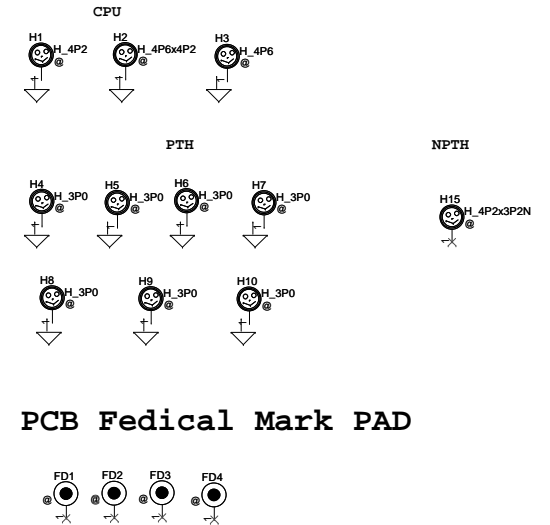
KEYBOARD CONN.



Card Reader + TP + Lid SW



Screw Hole



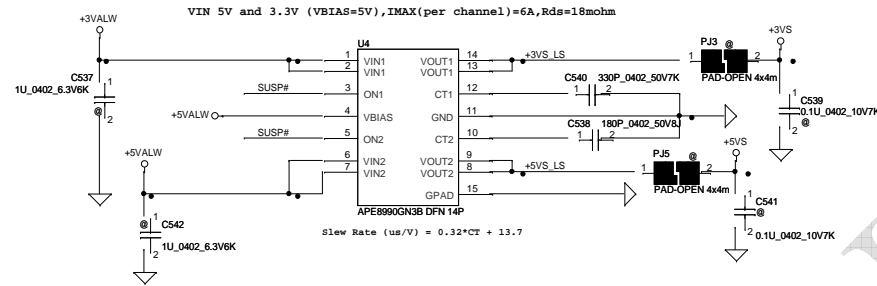
PCB Fedcal Mark PAD

ISPD

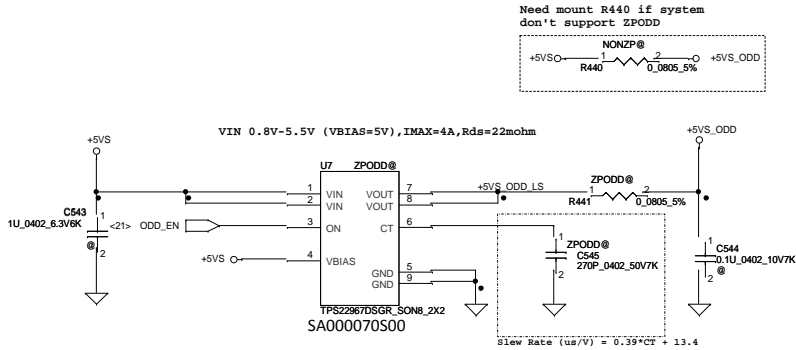
DA600152000
PCB LA-B412P

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| | | | | Date: Wednesday, January 22, 2014 Sheet 31 of 41 |

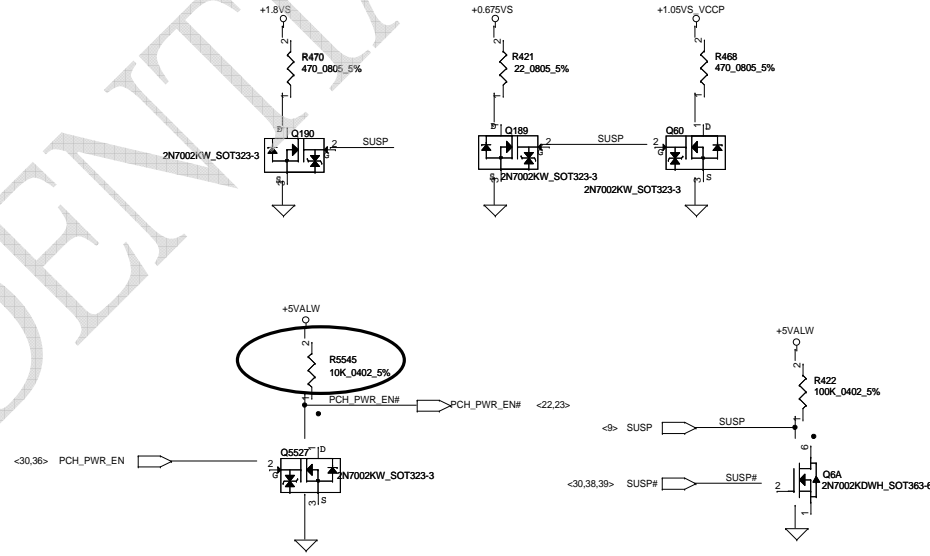
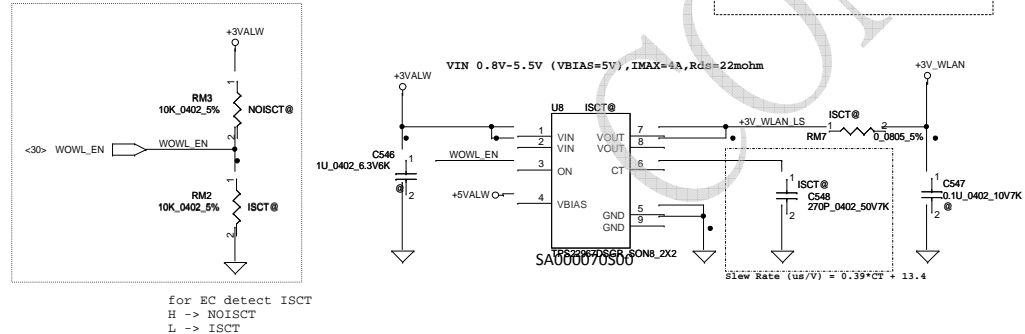
+5VALW TO +5VS
+3VALW TO +3VS
Load switch



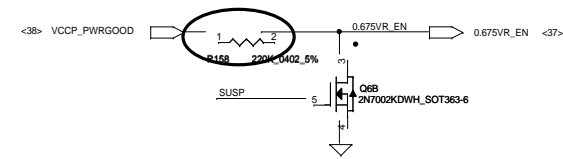
+5VS TO +5VS_ODD



+3VALW TO +3V_WLAN
for ISCT



For S3 CPU Power Saving

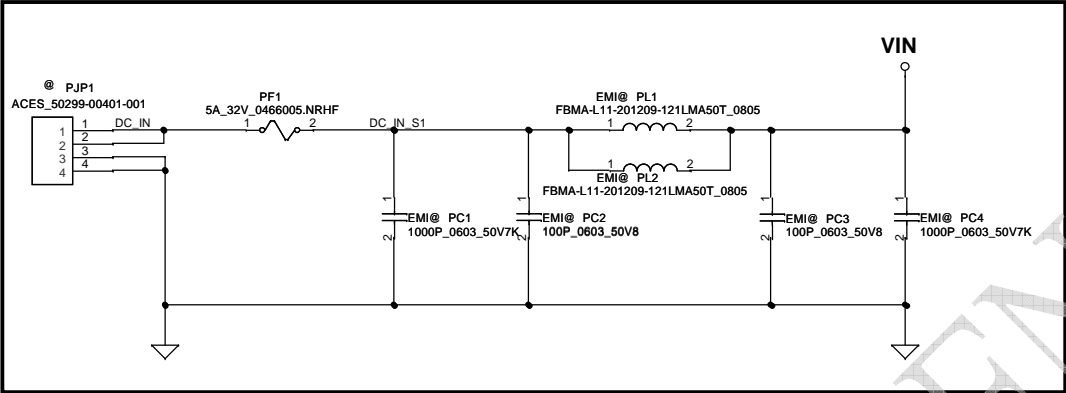


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Mark Green frame that means this part is not belong to layout module part .

Function Field :

Support 37.1
RTC 38.2
EMI Part 47.1



| | | | | | |
|---|------------|--------------------|------------|--------------------------|-----------------------------|
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| | | | | A3 | 0.2 |
| | | | | Document Number | LAB412P |
| | | | | Date | Wednesday, January 22, 2014 |
| | | | | Sheet | 33 of 41 |

Module model information

BQ24735A_V1.mdd

BQ24735A_V2.mdd

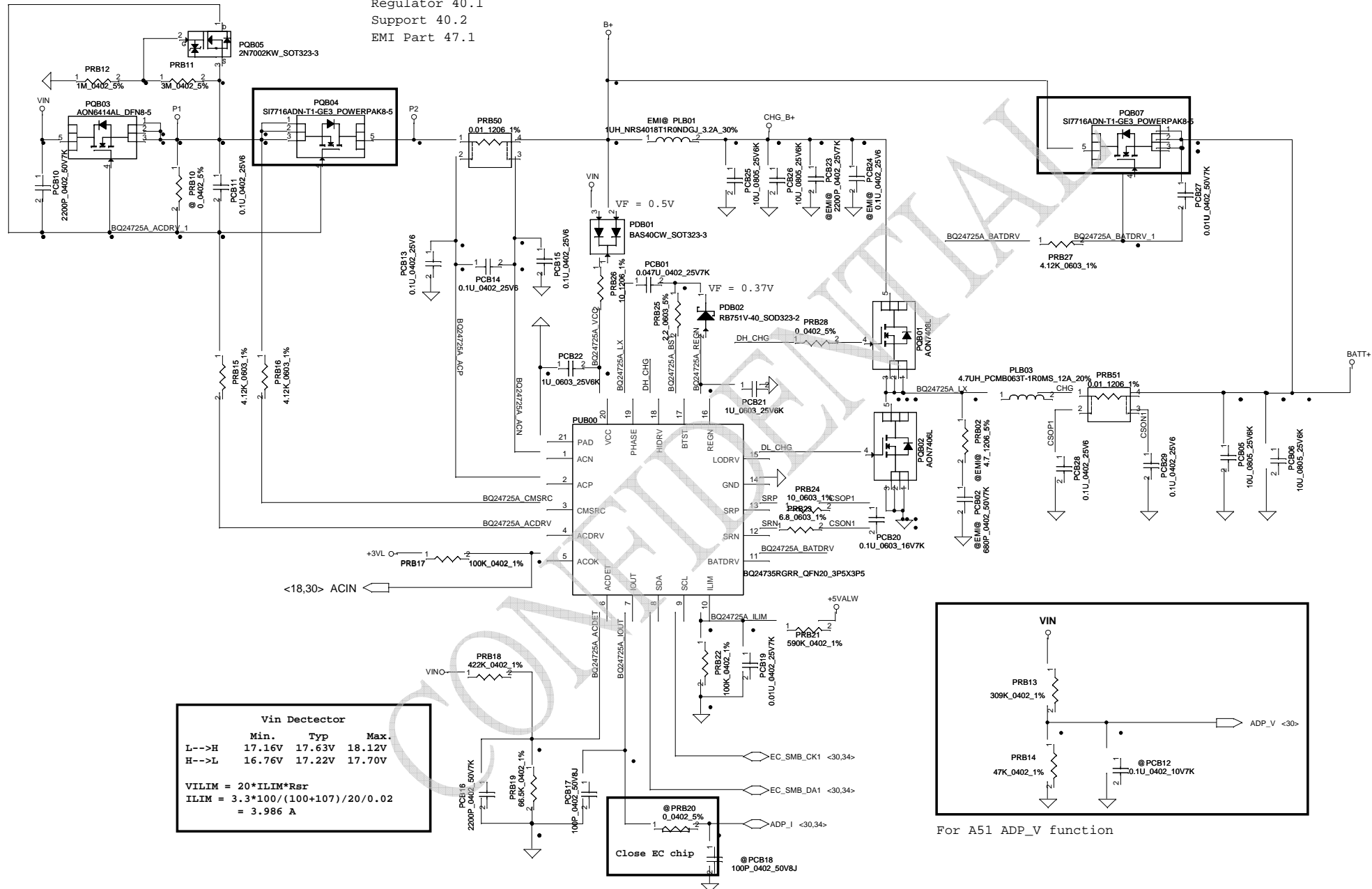
Mark Green frame that means this part is not belong to layout module part .

Function Field :

Regulator 40.1

Support 40.2

EMI Part 47.1



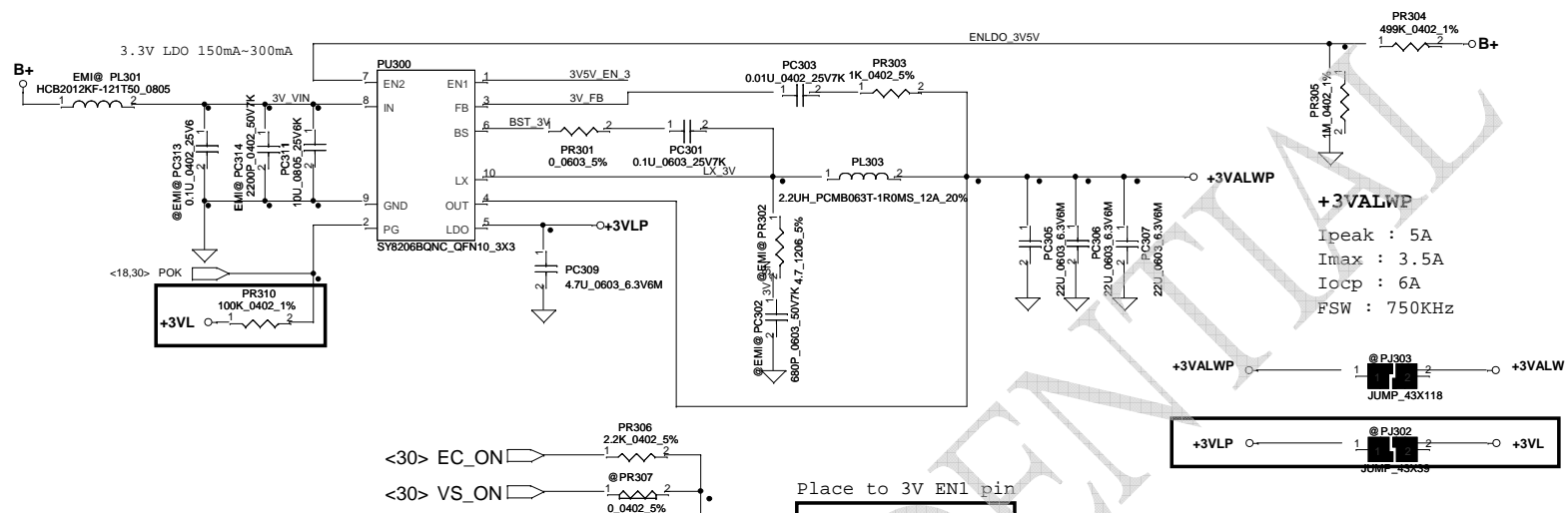
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SY8206B_V2.mdd

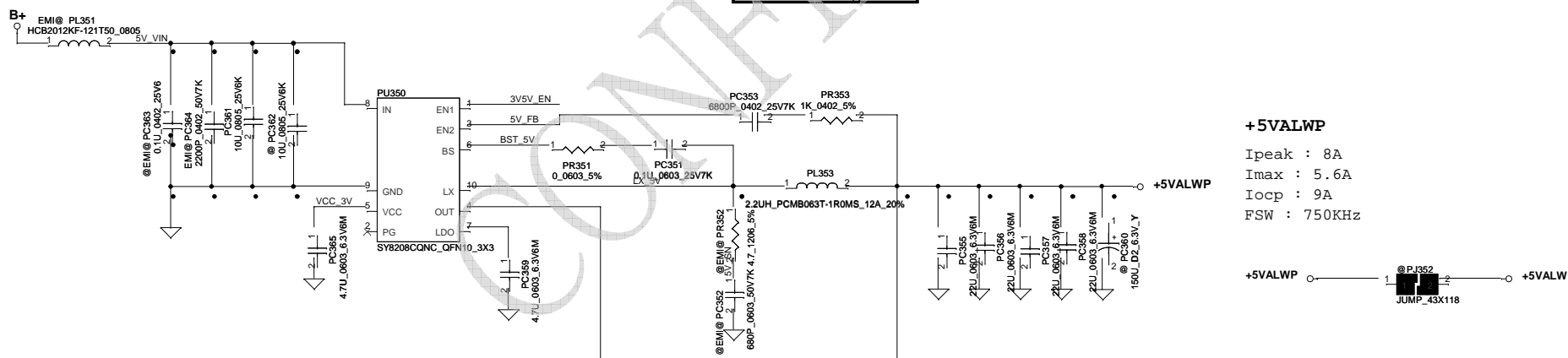
Function Field :

Support 35.2

EMI Part 47.1



SY8208C_V2.mdd



| | | | | | | |
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| | | | | Document Number | Rev 0.2 | |
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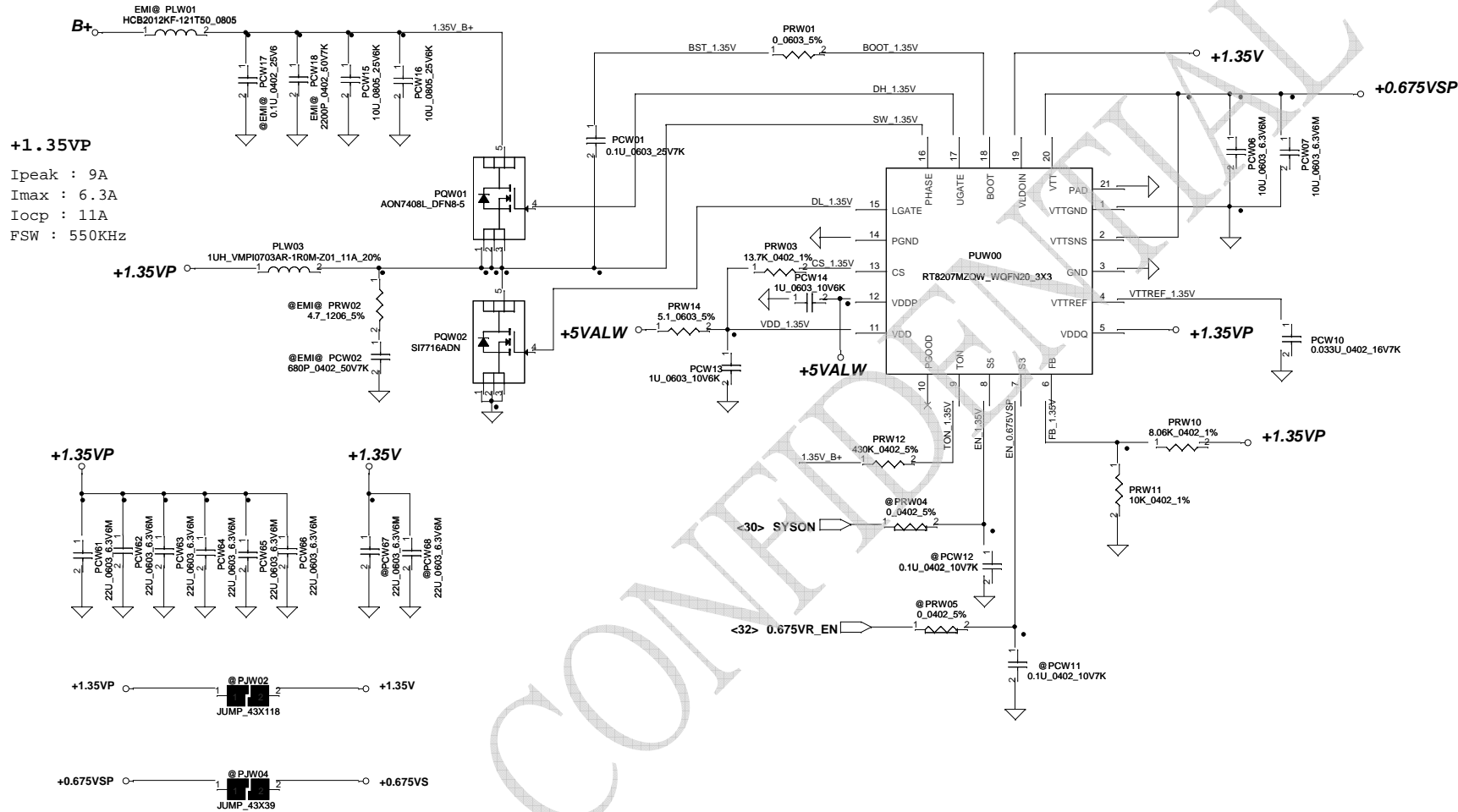
Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Mark Green frame that means this part is not belong to layout module part .

Function Field :

Regulator 35.3
Support 35.4
EMI Part 47.1



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| Issued Date | 2013/11/26 | Deciphered Date | 2014/11/26 | Title |
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| | | | | 0.2 |
| | | | | LAB412P |
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Module model information

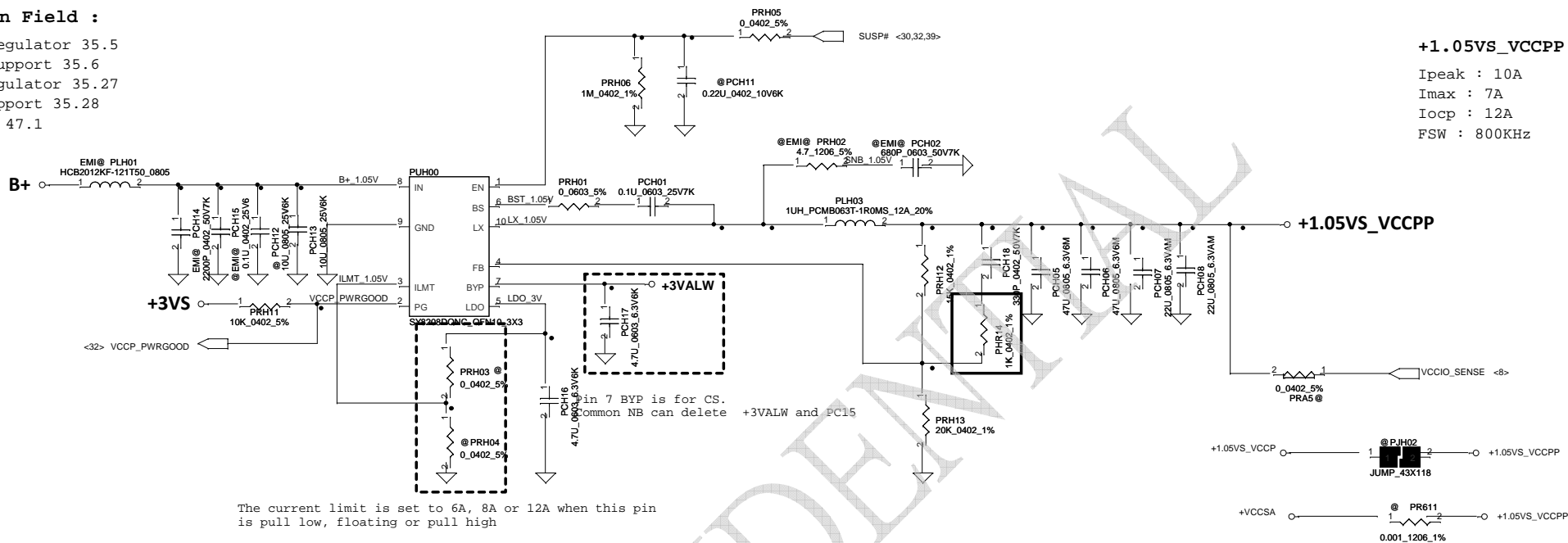
SY8033_V1.mdd

Mark Green frame that means this part is not belong to layout module part .

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2

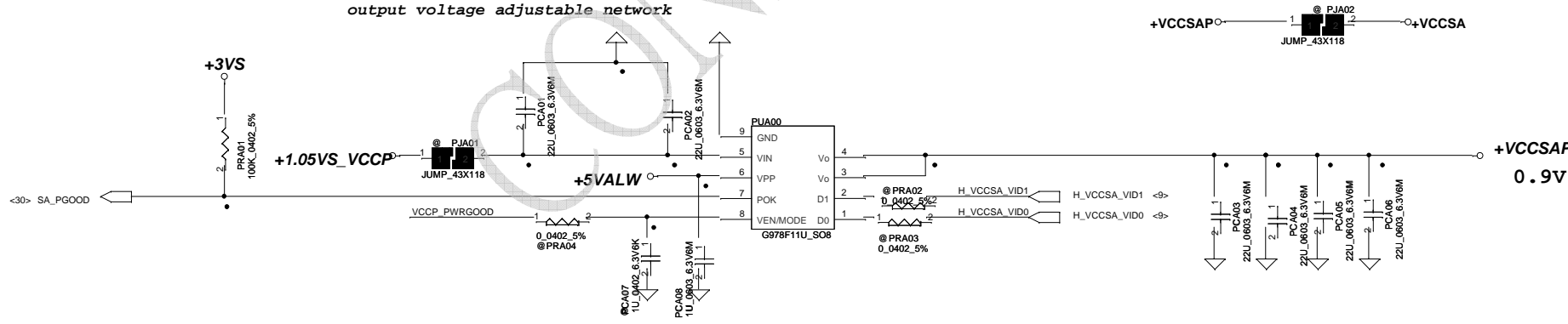
Function Field :

- +1.05V Regulator 35.5
- +1.05V Support 35.6
- +1.0V Regulator 35.27
- +1.0V Support 35.28
- EMI Part 47.1



| VID [0] | VID[1] | VCCSA Vout |
|---------|--------|------------|
| 0 | 0 | 0.9V |
| 0 | 1 | 0.85V |
| 1 | 0 | 0.775V |
| 1 | 1 | 0.75V |

output voltage adjustable network



| | | | | |
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| | | | | Date: Wednesday, January 22, 2014 |
| | | | | Sheet 38 of 41 |

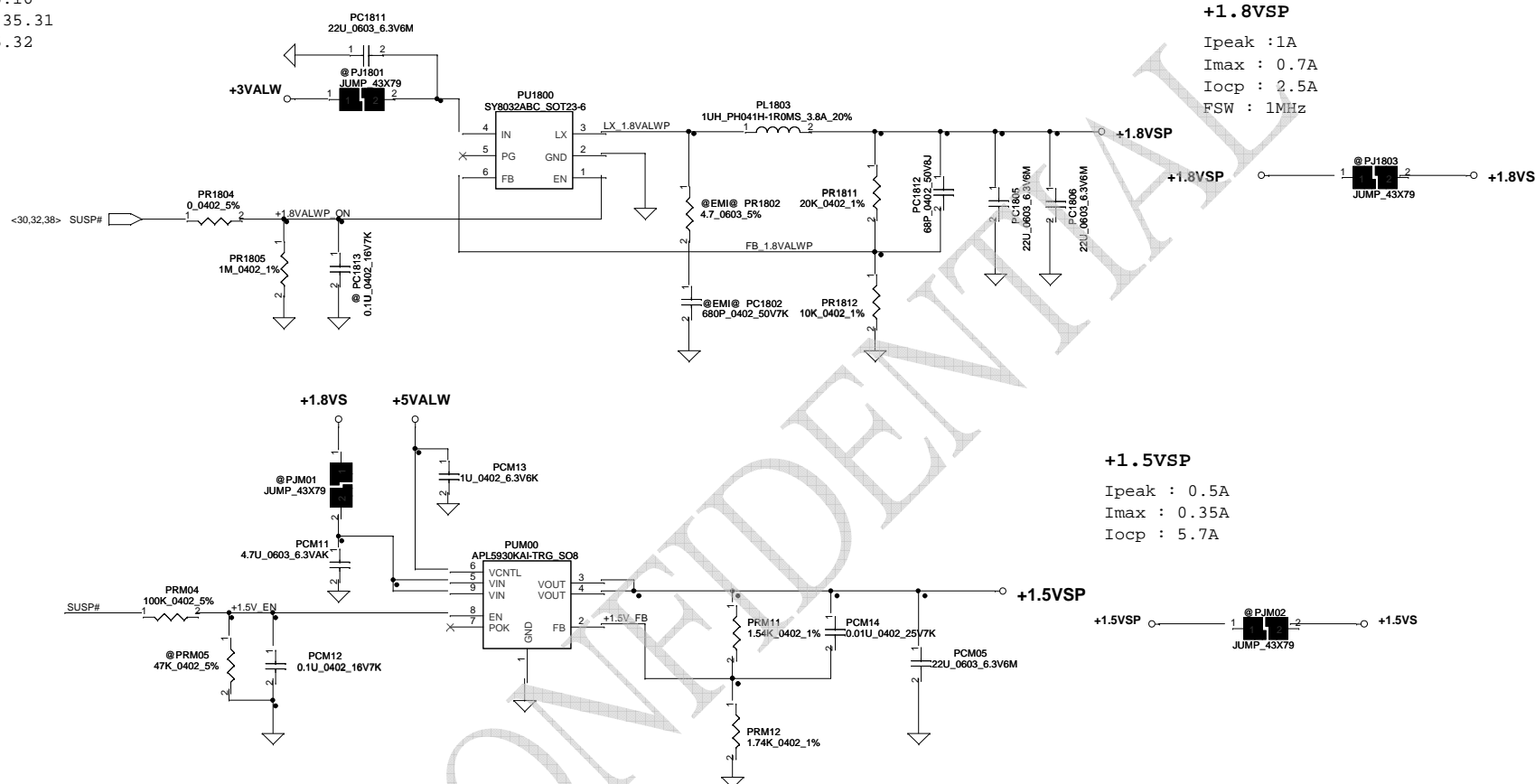
Module model information

SY8033_V1.mdd

Mark Green frame that means this part is not belong to layout module part .

Function Field :

+1.8V Regulator 35.15
+1.8V Support 35.16
+1.5V Regulator 35.31
+1.5V Support 35.32
EMI Part 47.1



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| | | | | LAB412P | 0.2 |
| | | | | Date | Wednesday, January 22, 2014 |
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ISL95833_V1B.mdd

1. The AL bulk capacitor of B+ should be very close to CPU_CORE MOSFET.
2. Input ceramic caps must place on symmetry same location on top side and bottom side.

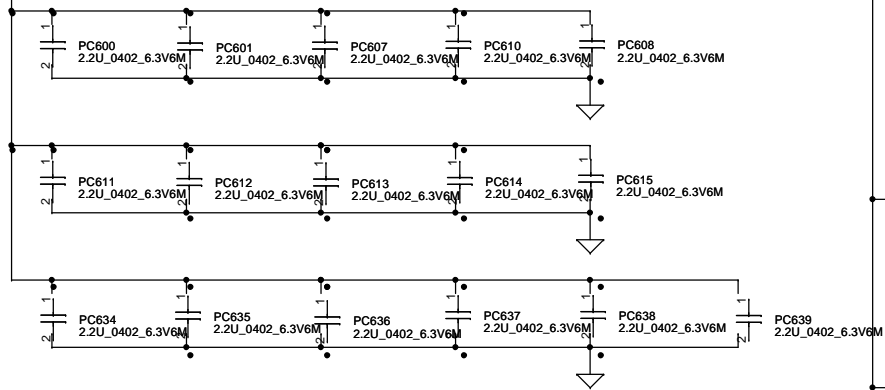
0.22uH DCR= 0.97+/-5% m ohm, Idc~Isat= 25~34A

+CF

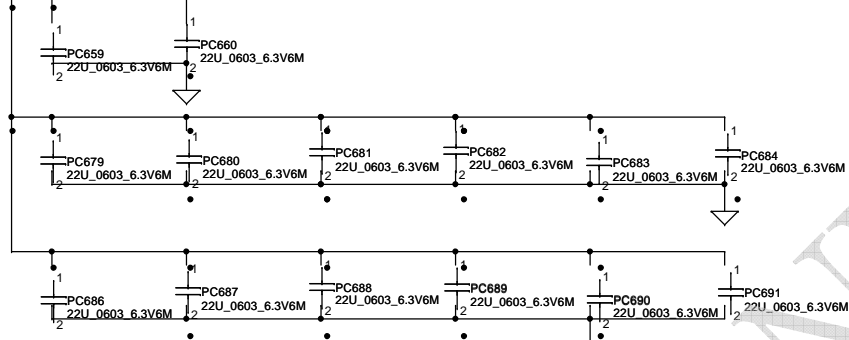
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|--|--------------------|-----------------|---------------------------------------|--------------------------|-----|
| Security Classification | Compal Secret Data | | Title | Compal Electronics, Inc. | |
| Issued Date | 2013/11/26 | Deciphered Date | 2014/11/26 | CPU/GFX CORE | |
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| | | | Created | 2013/11/26 | 01 |

CPU_Core output CAP (Including MLCC) 36.4

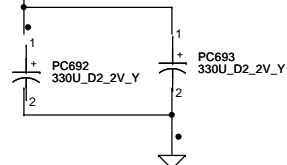
+CPU_CORE



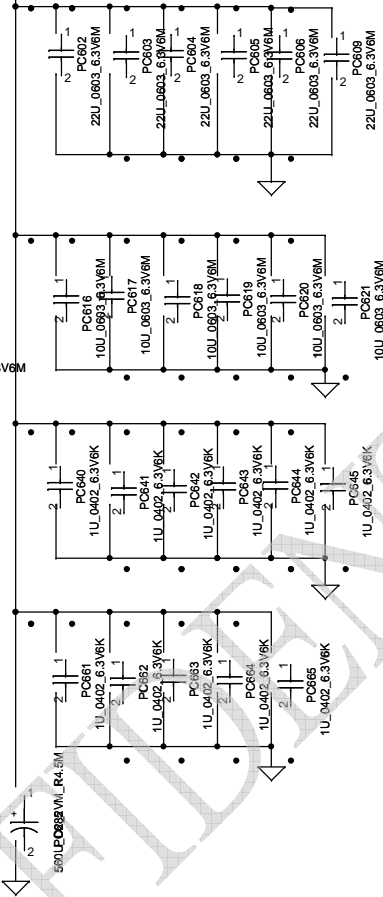
+CPU_CORE



+CPU_CORE



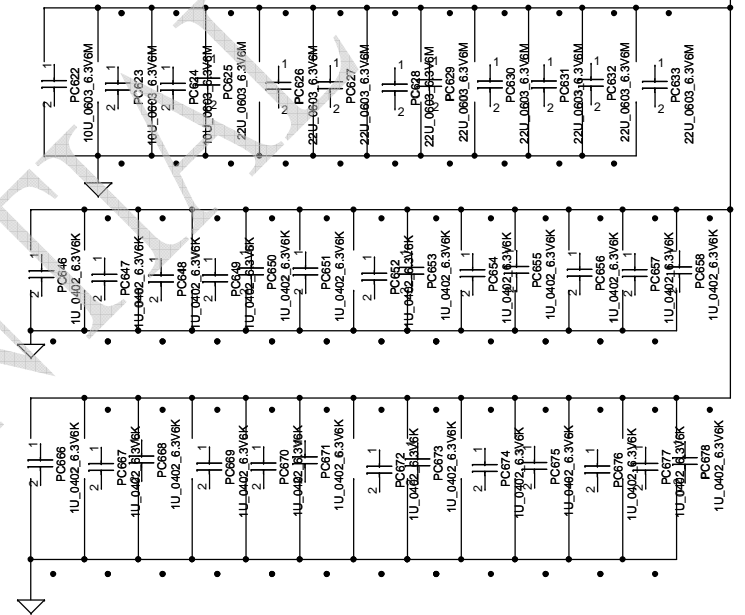
+GFX_CORE



GFX output CAP (Including MLCC) 36.5

VCCP output Cap (Including MLCC) 36.6

+1.05VS_VCCP



| | | | | | | | |
|-----------------|----------|------|------|-------|-----|-------|-------|
| Chief River ULV | 330uF*9m | 22uF | 10uF | 2.2uF | 1uF | 470uF | 560uF |
| CPU | 2 | 14 | | 16 | | | |
| GFX_CORE | | 6 | 6 | | 11 | | 1 |
| 1.05V_VCCP | | 9 | 3 | | 26 | | |

| | | | | | | | | | | | |
|---|--|--------------------|--|---------------------------------|--|------------|--|-----------------------------------|-----------------------------|-------|----------|
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| | | | | | | | | Date: | Wednesday, January 22, 2014 | Sheet | 41 of 41 |
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